A General Analysis of Passive Component Sizing for Input Inductor Buck Converters

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***Abstract*—Converters that incorporate split inductor designs demonstrate great potential for delivering high power while maintaining compact sizes, making them well-suited for data center applications. The input inductor buck converter, incorporating split inductors on the input side, represents the most fundamental topology with the split inductor design. This work presents a comprehensive analysis of the input inductor buck converter, deriving analytical expressions for bypass capacitor voltage and input inductor currents. Simulation and experimental results are provided to validate the analysis. The proposed model serves as a tool for designers to determine optimal component values based on passive volume and switch stress constraints.**

***Index Terms*—split inductor, input inductor buck converter, current source buck converter**

I. Introduction

The design criteria for point-of-load (PoL) converters in data centers prioritize high power delivery capabilities [1] and compact sizes. Recent studies have demonstrated that split inductor designs merged with hybrid switched-capacitor converters (SCCs) enable high power density [2] and lay the foundation for future implementation in system-in-package (SiP) or system-on-chip (SoC) solutions [3]. While split inductors can be embedded into various complex designs, one of the most fundamental topologies utilizing split inductors is the input inductor buck converter, or current source buck converter [4] [5], as illustrated in Fig. 1(a). By incorporating split inductors on the input side, this converter offers several potential advantages, including reduced electromagnetic interference (EMI) filter size and inductor current stress [6].

Although interest in split inductor converters continues to rise, limited research has been conducted on the bypass capacitor associated with the split inductors (C_b in Fig. 1). Previous studies on input inductor buck converters commonly assume linear current waveforms for both inductors [7]. While such modeling facilitates a general understanding of the converter behavior, its assumptions inherently lead to negligible voltage ripple across the bypass capacitor, preventing this model from being well-suited for passive component sizing. The uncharacterized capacitor voltage ripple also leads to non-optimal design choices for other components, such as switches whose peak stresses are directly related to the maximum bypass capacitor voltage ripple.

This work presents a comprehensive model of the split inductor buck converter which includes both inductor and capacitor ripple. The remainder of this work is organized as follows. Section II presents a comprehensive analysis of the input inductor buck converter, deriving a general expression for the bypass capacitor voltage, which remains applicable under varying conditions such as switching frequency, output power, and mismatched inductance values. In Section III, experimental results are provided to verify the accuracy of the model. Based on the validated model, Section IV analyzes trade-offs when selecting passive components and the switches. The analysis presented in this work establishes a foundation for potential extension to other topologies that incorporate split inductors, thereby supporting future analysis to optimize split inductor converters for numerous applications.

II. Theoretical Analysis

To ensure the accuracy of the model, the ripple of the output voltage is assumed to be negligible such that the output voltage is a constant, V_{out}. Power losses are also neglected in the analysis for simplicity. The voltage across the bypass capacitor is represented as a time-dependent function, $v_{C_b}(t)$. Moreover, two phase operation is assumed for the input inductor buck converter here, and the converter's behavior in each phase is analyzed separately in the following two subsections.

A. Phase One

As shown in Fig. 1(b), when S_H is conducting, the inductor voltages can be described as $V_{L_t,1} = V_{in} - V_{out}$ and $v_{L_b,1}(t) = v_{C_b,1}(t) - V_{out}$. The constitutive equation of a capacitor describes the current flowing through the bypass capacitor, $i_{C_b}(t)$, to be written in terms of $v_{C_b}(t)$. Since the current through the bottom inductor, $i_{L_b}(t)$, flows only into C_b in phase one, $i_{L_b}(t)$ is also directly related to $v_{C_b}(t)$. Thus, in addition to the representation shown before, the voltage of the bottom inductor, $v_{L_b,1}(t)$, can be expressed as

$$\begin{aligned} v_{L_b,1}(t) &= L_b \frac{di_{L_b,1}(t)}{dt} \\ &= -L_b \frac{di_{C_b,1}(t)}{dt} \\ &= -C_b L_b \frac{d^2 v_{C_b,1}(t)}{dt^2}. \end{aligned} \tag{1}$$

Combining $v_{L_b,1}(t) = v_{C_b,1}(t) - V_{out}$ and (1) yields

$$C_b L_b \frac{d^2 v_{C_b,1}(t)}{dt^2} + v_{C_b,1}(t) - V_{out} = 0. \tag{2}$$

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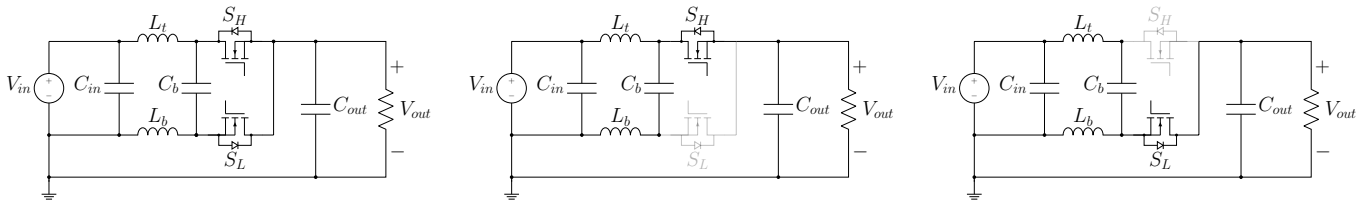


(a) (b) (c)

Fig. 1: (a) Schematic of the input inductor buck converter, indicating (b) phase one operation and (c) phase two operation.

This is a second-order linear ordinary differential equation, and the corresponding solution with free parameters k_1 and k_2 is

$$v_{C_b,1}(t) = \sqrt{{k_1}^2 + {k_2}^2}\cos\left(\frac{1}{\sqrt{C_b L_b}}t - \tan^{-1}(\frac{k_2}{k_1})\right) + V_{out}. \quad (3)$$

Thus, the general behavior of the bypass capacitor voltage can be described by a cosine function. To simplify the expression, $V_{pk,1}$ is introduced to represent the amplitude of the cosine waveform, and θ_1 is a parameter associated with the phase shift:

$$v_{C_b,1}(t) = V_{pk,1}\cos(\frac{1}{\sqrt{C_b L_b}}t + \theta_1) + V_{out}. \quad (4)$$

Since the bypass capacitor voltage is modeled to optimize passive component sizing, $V_{pk,1}$, θ_1, and V_{out} are treated as unknowns that can be determined based on given operating conditions and component values. According to (4), the resonant frequency of phase one is $\omega_1 = \frac{1}{\sqrt{C_b L_b}}$, which aligns with the resonant frequency analysis of the associated LC tank. In phase one, the voltage across the top inductor is constant, as shown in Fig. 1(b), and therefore can be treated as ac short. As a result, L_t does not contribute to the resonant frequency during phase one.

With phase durations defined as

$$t_1 = DT_{sw},\ t_2 = (1-D)T_{sw}, \quad (5)$$

the bypass capacitor waveform for phase one can be represented as a segment of length t_1 extracted from $v_{C_b,1}(t)$ waveform, as illustrated in Fig. 2. Here, $V_{pk,1}$ is assumed to be positive for clearer visualization. Given that $v_{C_b,1}(t)$ is a sinusoidal function, the time interval of phase one is chosen as $[-\frac{t_1}{2}, \frac{t_1}{2}]$ to simplify the calculation.

B. Phase Two

Similarly, during phase two, the bypass capacitor voltage can be expressed as

$$v_{C_b,2}(t) = V_{pk,2}\cos(\frac{1}{\sqrt{C_b L_t}}t + \theta_2) + V_{in} - V_{out}, \quad (6)$$

where the respective resonant frequency is given by $\omega_2 = \frac{1}{\sqrt{C_b L_t}}$. In this phase, $V_{L_b,2} = -V_{out}$ and $v_{L_t,2}(t) = V_{in} - V_{out} - v_{C_b,2}(t)$. The time interval of phase two is $[-\frac{t_2}{2}, \frac{t_2}{2}]$

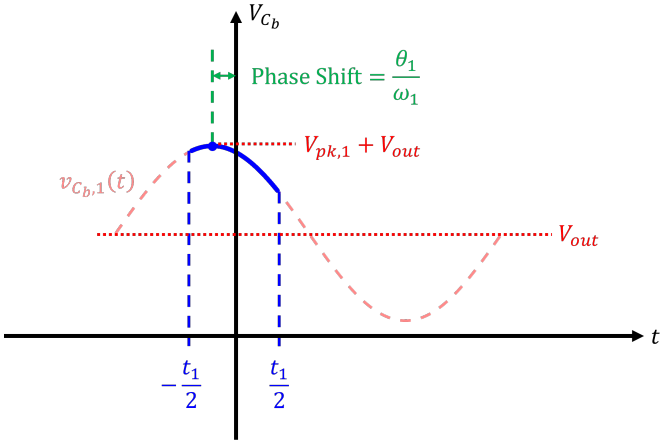


Fig. 2: A visualization of $v_{C_b,1}(t)$.

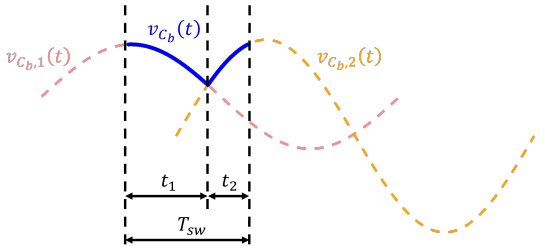


Fig. 3: The bypass capacitor voltage waveform over a period. As shown, $v_{C_b}(t)$ is the combination of the waveforms of two states, $v_{C_b,1}(t)$ and $v_{C_b,2}(t)$.

correspondingly. The values of $V_{pk,2}$ and θ_2 will be discussed in the next subsection.

C. Derivation of Equations

To determine the capacitor voltage in both phases, the five unknowns ($V_{pk,1}$, $V_{pk,2}$, θ_1, θ_2, and V_{out}) must be solved utilizing five equations derived from the topology. Note, $V_{pk,1}$ and $V_{pk,2}$ are assumed to be positive for the following analysis.

Based on the periodic steady-state analysis, the average voltage across an inductor over a complete period is zero, resulting in two equations for the two input inductors. The simplified equations for L_t and L_b respectively are

$$\frac{2V_{pk,2}}{\omega_2}\sin(\omega_2\frac{t_2}{2})\cos(\theta_2) = (V_{in} - V_{out})t_1, \quad (7)$$

$$\frac{2V_{pk,1}}{\omega_1}\sin(\omega_1\frac{t_1}{2})\cos(\theta_1) = V_{out}t_2. \quad (8)$$

Additionally, the overall behavior of $v_{C_b}(t)$ can be described as the combination of $v_{C_b,1}(t)$ and $v_{C_b,2}(t)$ waveforms over a period as depicted in Fig. 3. Voltage continuities of $v_{C_b}(t)$ between the two phases lead to

$$V_{pk,1}\cos(\omega_1\frac{t_1}{2}+\theta_1)+V_{out}=V_{pk,2}\cos(\omega_2\frac{-t_2}{2}+\theta_2)+V_{in}-V_{out}, \tag{9}$$

$$V_{pk,1}\cos(\omega_1\frac{-t_1}{2}+\theta_1)+V_{out}=V_{pk,2}\cos(\omega_2\frac{t_2}{2}+\theta_2)+V_{in}-V_{out}. \tag{10}$$

The sum of the average current through each inductor is equal to the average output current. For each inductor, the inductor voltage is a constant in one phase and a cosine function in the other phase, resulting in inductor currents that are linear in one phase and sinusoidal in the other. The average output current can be written as

$$\begin{aligned} I_{out} &= \frac{1}{T}\Big(\int_{\frac{-t_1}{2}}^{\frac{t_1}{2}} i_{out,1}(t)\,dt+\int_{\frac{-t_2}{2}}^{\frac{t_2}{2}} i_{out,2}(t)\,dt\Big)\\ &= \frac{1}{T}(I_1+I_2), \end{aligned} \tag{11}$$

where I_1 and I_2 are parameters defined as follows:

$$\begin{aligned} I_1 = \frac{V_{in}-V_{out}}{2L_t}{t_1}^2 - V_{pk,2}C_b\omega_2 t_1\sin(\omega_2\frac{t_2}{2}+\theta_2)\\ +2V_{pk,1}C_b\sin(\omega_1\frac{t_1}{2})\sin(\theta_1), \end{aligned} \tag{12}$$

$$\begin{aligned} I_2 = \frac{-V_{out}}{2L_b}{t_2}^2 + V_{pk,1}C_b\omega_1 t_2\sin(\omega_1\frac{t_1}{2}+\theta_1)\\ -2V_{pk,2}C_b\sin(\omega_2\frac{t_2}{2})\sin(\theta_2). \end{aligned} \tag{13}$$

In summary, five equations (7)-(11) are derived to solve for five unknowns: $V_{pk,1}$, $V_{pk,2}$, θ_1, θ_2, and V_{out}. Given predefined values for input voltage, output load, passive components, duty ratio, and switching frequency, the exact analytical expression for the bypass capacitor voltage can be derived. This model applies to various operating conditions, including switching frequencies that range from around resonance to well above resonance. As illustrated in Fig. 4, PLECS simulation waveforms exhibit strong alignment with theoretical calculations, thereby validating the proposed model.

D. Output Voltage

If the inductor currents are assumed to be linear, the output voltage can be expressed as $V_{out} = DV_{in}$. However, the analytical expression derived in this work provides an exact calculation of the output voltage as

$$V_{out} = V_{in}\frac{\frac{t_1\omega_2}{\tan(\omega_2\frac{t_2}{2})}+2}{\frac{t_2\omega_1}{\tan(\omega_1\frac{t_1}{2})}+\frac{t_1\omega_2}{\tan(\omega_2\frac{t_2}{2})}+4}. \tag{14}$$

This suggests that V_{out} is a function of the two resonant frequencies, the switching frequency, and the duty ratio described in (5). To strengthen the key influencing factors and reduce the number of variables, two parameters, α and β, are introduced to characterize the relationship between the resonant frequencies and the switching frequency.

$$\alpha = \frac{\omega_{sw}}{\omega_1} = \omega_{sw}\sqrt{L_bC_b}, \tag{15}$$

$$\beta = \frac{\omega_{sw}}{\omega_2} = \omega_{sw}\sqrt{L_tC_b}. \tag{16}$$

Combining (14)-(16) leads to

$$V_{out} = V_{in}\frac{\frac{\frac{2\pi D}{\beta}}{\tan(\frac{\pi(1-D)}{\beta})}+2}{\frac{\frac{2\pi(1-D)}{\alpha}}{\tan(\frac{\pi D}{\alpha})}+\frac{\frac{2\pi D}{\beta}}{\tan(\frac{\pi(1-D)}{\beta})}+4}. \tag{17}$$

In the special cases where $\alpha = \beta$ and $D = \frac{1}{2}$, (17) is equivalent to $V_{out} = DV_{in}$. However, V_{out} is more accurately

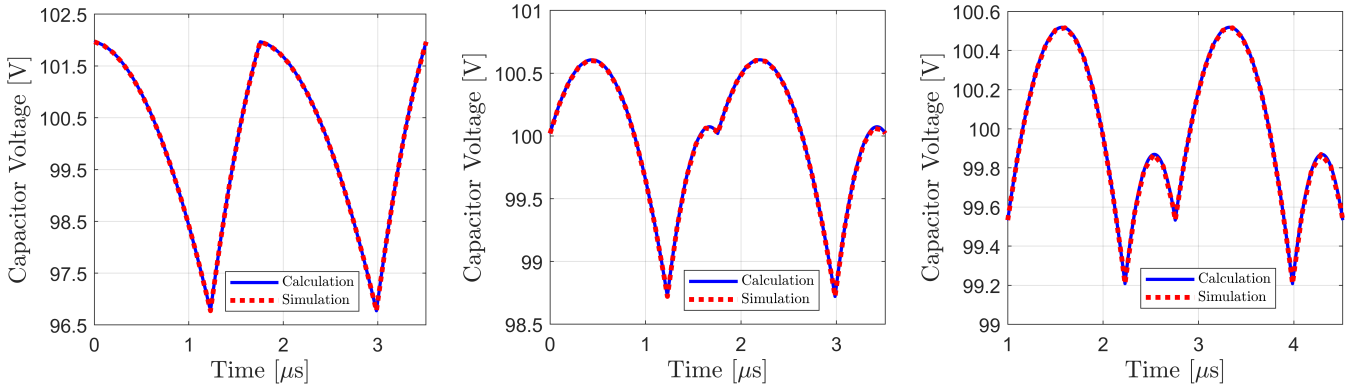
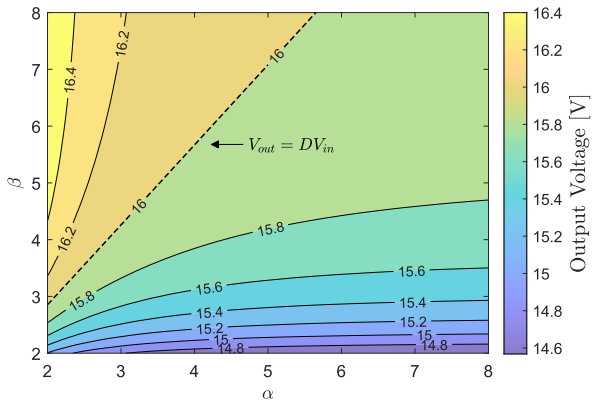
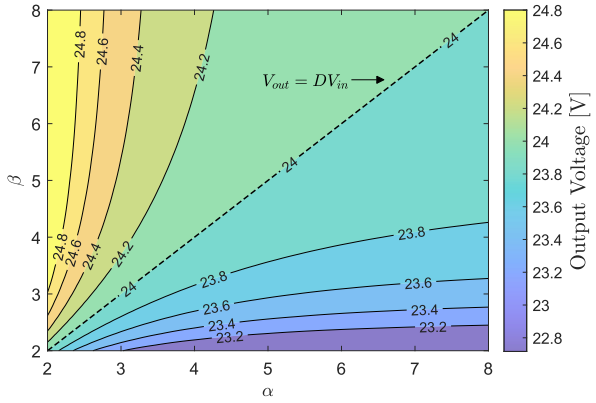


Fig. 4: Calculated and simulated capacitor voltage wavefroms under three different output powers. The values of passive components are $L_t = L_b = 5$ μH and $C_b = 1$ μF. The operating conditions are $V_{in} = 100$ V, $D = 0.7$, and $f_{sw} = 8f_{res}$. The output loads and powers are: (a) $R = 5$ Ω, $P_{out} \approx 983$ W; (b) $R = 20$ Ω, $P_{out} \approx 246$ W; (c) $R = 80$ Ω, $P_{out} \approx 61$ W.



(a)



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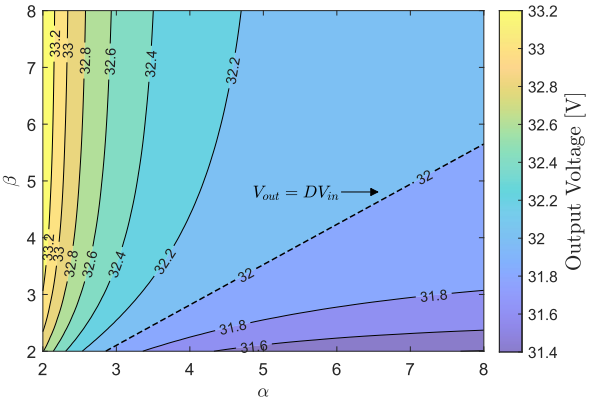


(c)

Fig. 5: Modeled variation in output voltage as a function of α and β. $V_{in} = 48$ V. The duty ratios are, respectively: (a) $D = \frac{1}{3}$, (b) $D = \frac{1}{2}$, and (c) $D = \frac{2}{3}$.

determined by the interdependence of α, β, and the duty ratio. As depicted in Fig. 5(a), when $D = \frac{1}{3}$, densely packed contour lines are observed in the region where α and β are relatively small. This indicates that slight variations in the resonant frequencies result in rapid changes in the output voltage. Notably, the dense contour lines appear approximately horizontal, suggesting that changes along the y-axis, which is β, have a more pronounced effect on the output than the changes along the x-axis, which is α. As both α and β becomes sufficiently large, (17) converges to DV_{in}. A similar analysis can be conducted for the other cases shown in Fig. 5(b) and Fig. 5(c), which correspond to a duty ratio of $\frac{1}{2}$ and $\frac{2}{3}$ respectively.

E. Bypass Capacitor Voltage Ripple

Although the average bypass capcaitor voltage is equal to V_{in}, the voltage ripple varies across different scenarios. Since the capacitor voltage influences the energy storage of passive components and thereby their sizing requirements, as well as the peak voltage stress across the switches, a careful analysis of the voltage ripple is essential to support optimal component choices.

The capacitor ripple voltage can be determined as the difference between its maximum and minimum values. For the cases of interest investigated in this paper, when I_{out} is positive and the converter operates in continuous-conduction mode (CCM), the minimum capacitor voltage is observed at the transition from phase one to phase two, as phase one generally corresponds to capacitor discharging and phase two corresponds to capacitor charging. The maximum voltage; however, needs to be determined based on operating conditions. Since the bypass capacitor voltage waveform comprises segments from two cosine functions corresponding to the two operating states, whether each segment contains the cosine peak or not determines the position of the maximum value. Specifically, if a segment contains a cosine peak, the capacitor voltage waveform in that state exhibits non-monotonic behavior, implying that the maximum value of the segment occurs at the peak; conversely, if no peak is present, the waveform of that state is monotonic and the maximum value occurs at the endpoint. Since there are two states and the behavior of each state needs to be considered, there are four potential cases as shown in Table I.

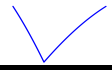
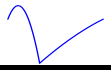
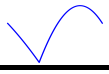
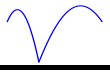
1) Determination of Cases: Given that the bypass capacitor voltage for phase one is $v_{C_b,1}(t) = V_{pk,1}\cos(\omega_1 t + \theta_1) + V_{out}$, the time at which the cosine function reaches its maximum is $t_{pk,1} = -\frac{\theta_1}{\omega_1}$. If $t_{pk,1}$ lies within the interval $[-\frac{t_1}{2}, \frac{t_1}{2}]$, the phase one waveform exhibits non-monotonic behavior; otherwise, it is monotonic. A similar analysis applies to state 2, where the determining condition depends on whether $t_{pk,2} = -\frac{\theta_2}{\omega_2}$ falls within $[-\frac{t_2}{2}, \frac{t_2}{2}]$.

2) Both Monotonic: For Case 1, when capacitor voltage waveforms for both phases are monotonic, the minimum and maximum happen at the end points of phases and the capacitor voltage ripples for each phase are

$$\begin{aligned}\Delta V_{C_b,pp,1} &= v_{C_b,1}(\frac{-t_1}{2}) - v_{C_b,1}(\frac{t_1}{2}) \\ &= V_{out} t_2 \omega_1 \tan(\theta_1),\end{aligned} \tag{18}$$

$$\begin{aligned}\Delta V_{C_b,pp,2} &= v_{C_b,2}(\frac{t_2}{2}) - v_{C_b,2}(\frac{-t_2}{2}) \\ &= -(V_{in} - V_{out}) t_1 \omega_2 \tan(\theta_2).\end{aligned} \tag{19}$$

TABLE I: Different cases of bypass capacitor voltage ripple.

	Case 1	Case 2	Case 3	Case 4
State 1	Monotonic	Non-Monotonic	Monotonic	Non-Monotonic
State 2	Monotonic	Monotonic	Non-Monotonic	Non-Monotonic
Waveforms				

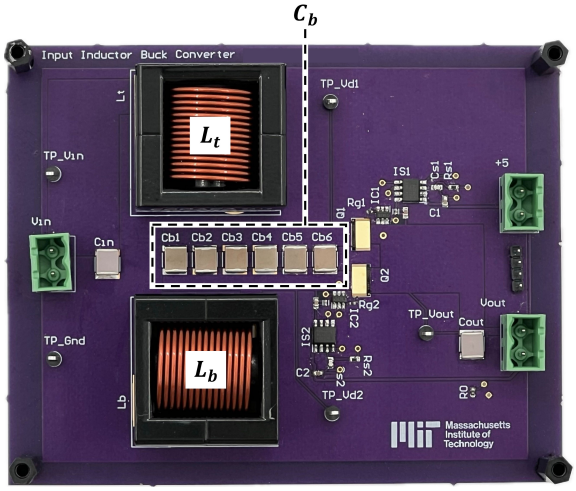


Fig. 6: Input inductor buck converter testbed.

TABLE II: Components selected for input inductor buck converter hardware prototype.

Component	Part Number	Description
$C_{b_{[1-6]}}$	C2220C473KFRACTU	0.047 μF
L_t, L_b	CPEX3231A-330MC	33 μH
S_H, S_L	GS61008T	100 V, 90 A
Gate Driver	LM5134BMF/NOPB	5 V
Isolator	ADUM5241	Power and Signal

Because of continuities between the two phases, the maximum voltage values for both phases are equivalent and

$$\Delta V_{C_b,pp} = \Delta V_{C_b,pp,1} = \Delta V_{C_b,pp,2}. \tag{20}$$

3) One Monotonic, One Non-Monotonic: For Case 2, the maximum voltage of phase two is $v_{C_b,2}(\frac{t_2}{2})$, while the peak voltage in phase one corresponds to the maximum value of the cosine waveform, expressed as $V_{pk,1}+V_{out}$. Since $V_{pk,1}+V_{out} > v_{C_b,1}(\frac{-t_1}{2}) = v_{C_b,2}(\frac{t_2}{2})$, the capacitor voltage ripple over a period is equal to the voltage ripple observed in phase one.

$$\begin{aligned}\Delta V_{C_b,pp} &= \Delta V_{C_b,pp,1} \\ &= \frac{1}{2} V_{out} t_2 \omega_1 \Big(\frac{1}{\sin(\omega_1 \frac{t_1}{2}) \cos(\theta_1)} \\ &\quad - \frac{1}{\tan(\omega_1 \frac{t_1}{2})} + \tan(\theta_1) \Big)\end{aligned} \tag{21}$$

Similar analysis can be conducted for Case 3 with

$$\begin{aligned}\Delta V_{C_b,pp} &= \Delta V_{C_b,pp,2} \\ &= \frac{1}{2}(V_{in} - V_{out}) t_1 \omega_2 \Big(\frac{1}{\sin(\omega_2 \frac{t_2}{2}) \cos(\theta_2)} \\ &\quad - \frac{1}{\tan(\omega_2 \frac{t_2}{2})} - \tan(\theta_2) \Big)\end{aligned} \tag{22}$$

4) Both Non-Monotonic: For Case 4, $\Delta V_{C_b,pp,1}$ is defined by (21), and $\Delta V_{C_b,pp,2}$ is given by (22). The overall bypass capacitor voltage ripple is determined by the larger of these two values.

III. Experimental Results

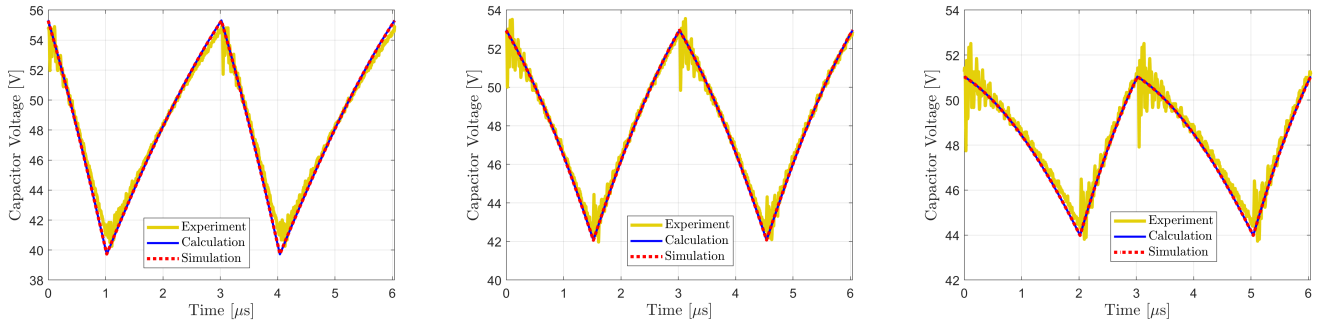
A testbed of the input inductor buck converter was built to verify the proposed model as shown in Fig. 6. The component selections are listed in Table II. The two input inductors have the same value, and the bypass capacitor is implemented using six parallel 0.047 μF capacitors. The hardware prototype is evaluated with $V_{in} = 48$ V under various duty cycles, power levels and switching frequencies.

A. Bypass Capacitor Voltage Verification

As illustrated in Fig. 7, to validate the accuracy of the proposed model under varying duty ratios, the converter is evaluated at duty ratios $D = \frac{1}{3}$, $\frac{1}{2}$, and $\frac{2}{3}$, with the load resistances appropriately adjusted to maintain a constant output power, P_{out}. It is observed that increasing the duty ratio results in a reduction of the bypass capacitor voltage ripple. This observation aligns with theoretical expectations, as a higher duty ratio under the same input voltage and output power leads to a lower bypass capacitor current. The accuracy of the proposed model is also validated by the close agreement between the experimental waveforms and the theoretical waveforms calculated using the model.

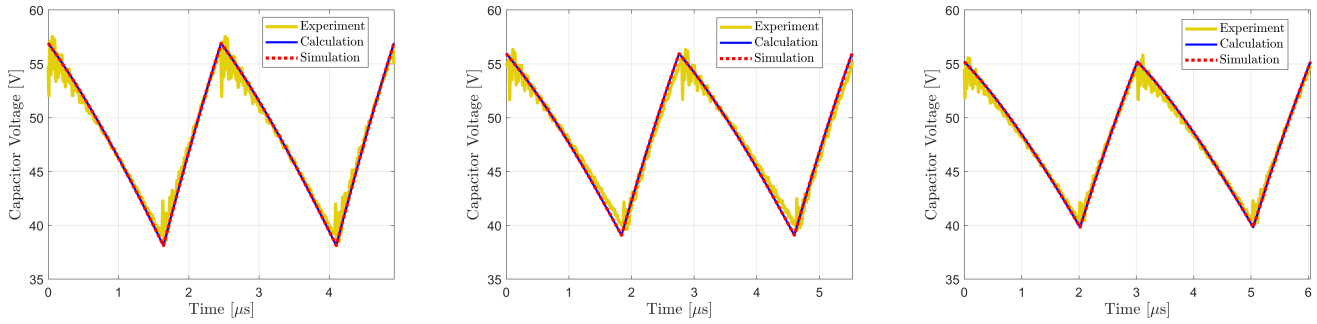
The hardware prototype can also be utilized to validate operation with different capacitance values. As depicted in Fig. 8, the experimental results closely align with the theoretical predictions, and the voltage ripple across the capacitor decreases as the bypass capacitance increases.

In all the verification cases discussed above, the selected switching frequency is 6.35 times the resonant frequency. To further evaluate the performance of the model when the switching frequency is equal to the resonant frequency, an



(a) (b) (c)

Fig. 7: Bypass capacitor voltage waveforms with different duty ratios. The switching frequency is $f_{sw} = 6.35 f_{res} = 331.13$ kHz. Given V_{in} = 48 V: (a) $D = \frac{1}{3}$, $V_{out} = 15.09$ V; (b) $D = \frac{1}{2}$, $V_{out} = 23.41$ V; (c) $D = \frac{2}{3}$, $V_{out} = 31.57$ V. Output loads are adjusted for P_{out} to be approximately 91 W.



(a) (b) (c)

Fig. 8: Bypass capacitor voltage waveforms with different capacitances: (a) $C_b = 0.188$ μF, $P_{out} \approx 188$ W; (b) $C_b = 0.235$ μF, $P_{out} \approx 190$ W; (c) $C_b = 0.282$ μF, $P_{out} \approx 192$ W. All the switching frequencies are approximately $f_{sw} = 6.35 f_{res}$. Given V_{in} = 48 V, $D = \frac{2}{3}$, and $R = 5$ Ω, the measured $V_{out} \approx 31$ V.

additional case is illustrated in Fig. 9. The experimental waveform exhibits a reasonably close alignment with the theoretical prediction. Since the low switching frequency leads to a large bypass capacitor voltage ripple, which results in increased power loss, the slight discrepancy between the experimental results and the model is due to the higher losses under this operating condition.

B. Output Voltage Verification

Additionally, the hardware prototype can be used to verify the output voltage relationship found in (17). To simplify the analysis, the inductors are equal such that $\alpha = \beta$.

When $D = \frac{1}{3}$, as illustrated in Fig. 10(a), V_{out} increases with the switching frequency and gradually converges to the asymptote $V_{out} = DV_{in}$ as α becomes sufficiently large. The largest discrepancy between the experimental data and the theoretical curve occurs near $\alpha \approx 1$, corresponding to the point of the lowest efficiency, therefore representing the most significant divergence from the ideal theoretical prediction. Overall, Fig. 10(a) demonstrates strong agreement between the experimental results and the theoretical analysis.

A similar analysis can be performed for the case with $D = \frac{2}{3}$ as depicted in Fig. 10(c). However, in this case, V_{out} decreases with increasing switching frequency and eventually converges to $V_{out} = DV_{in}$ as α becomes large enough. Additionally, when $D = \frac{1}{2}$, as illustrated in Fig. 10(b), V_{out} is always equivalent to DV_{in} regardless of the value of α. The experimental results for these two cases also exhibit close

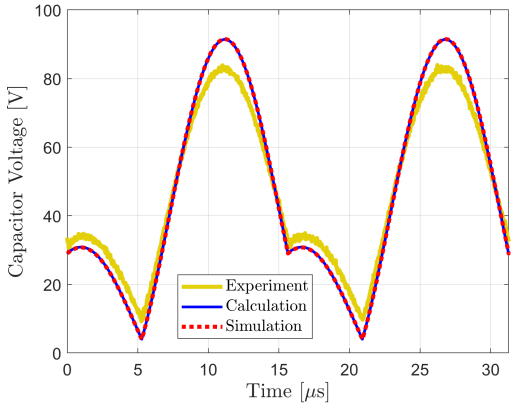
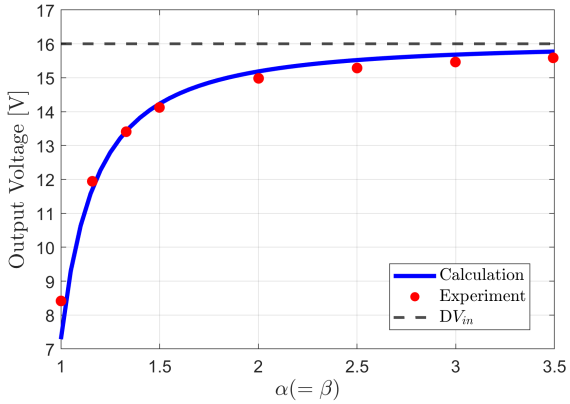
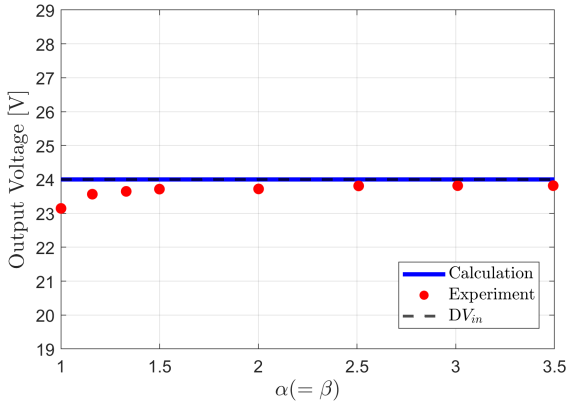


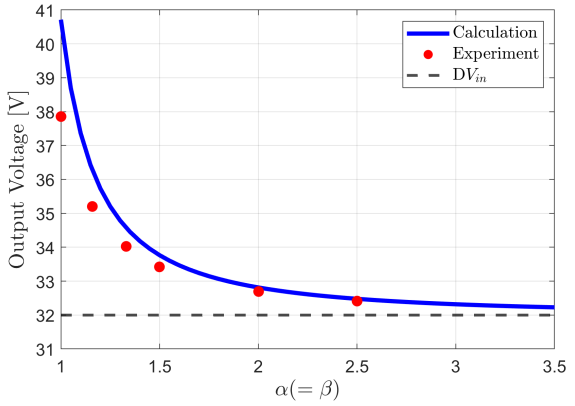
Fig. 9: Bypass capacitor voltage waveform with $f_{sw} \approx f_{res}$. Given V_{in} = 48 V, $D = \frac{1}{3}$, $C_b = 0.188$ μF, and $R \approx 9.83$ Ω, the measured $V_{out} \approx 8.42$ V with $P_{out} \approx 7.21$ W and $P_{in} \approx 12$ W.



(a)



(b)



(c)

Fig. 10: Output voltage measurement with varying switching frequencies. $V_{in} = 48$ V and (a) $D = \frac{1}{3}$, $R \approx 10\ \Omega$; (b) $D = \frac{1}{2}$, $R \approx 22.5\ \Omega$; (c) $D = \frac{2}{3}$, $R \approx 40\ \Omega$.

alignment with the theoretical model.

IV. Passive Component Volume

Building on the presented analysis and validation, the proposed model can be used to aid designers in selecting passive component values. The focus of this section is on minimizing passive component volume. It is assumed that the energy density of the bypass capacitor, $\rho_{E,C}$, is approximately 100 times that of the input inductors, $\rho_{E,L}$ [8]. The total volume of the passive components, $\mathrm{Vol_{tot}}$, is defined as the sum of the bypass capacitor volume, $\mathrm{Vol_{C_b}}$, and the input inductors volumes, $\mathrm{Vol_{L_t}}$ and $\mathrm{Vol_{L_b}}$. Each passive component's volume is calculated with its stored energy (E_{C_b}, E_{L_t} and E_{L_b}) and its corresponding energy density.

$$\begin{aligned}\mathrm{Vol_{tot}} &= \mathrm{Vol_{C_b}} + \mathrm{Vol_{L_t}} + \mathrm{Vol_{L_b}} \\ &= \frac{E_{C_b}}{\rho_{E,C}} + \frac{E_{L_t} + E_{L_b}}{\rho_{E,L}}.\end{aligned} \tag{23}$$

As $\rho_{E,C} = 100\rho_{E,L}$, (23) can be simplified to

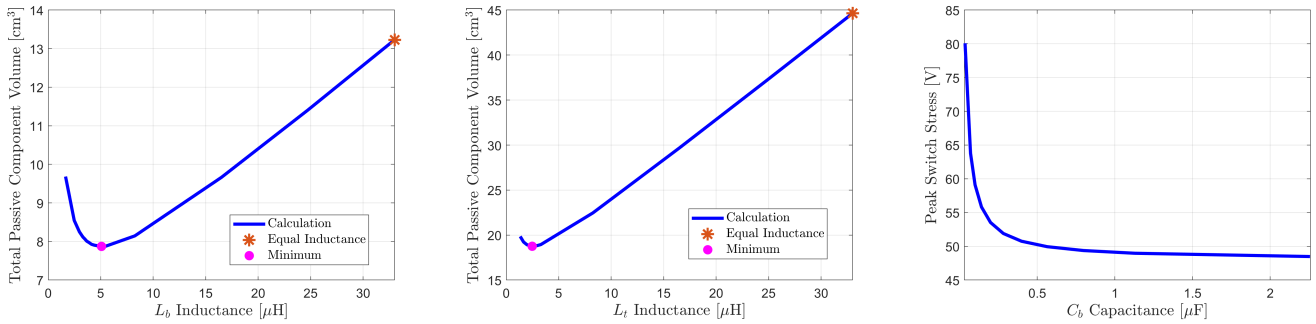
$$\mathrm{Vol_{tot}} = \frac{1}{\rho_{E,L}}\left(\frac{E_{C_b}}{100} + E_{L_t} + E_{L_b}\right). \tag{24}$$

If $\rho_{E,L}$ is treated as a constant, minimizing the total passive component volume is equivalent to minimizing the expression $\frac{E_{C_b}}{100} + E_{L_t} + E_{L_b}$. Note, this analysis does not consider the scaling laws of passive components [9].

The peak capacitor voltage and inductor currents are necessary for calculating the energy stored in the passive components. Based on the derived bypass capacitor voltage expression, the maximum capacitor voltage can be determined. Additionally, the expressions for the inductor currents can be formulated as $i_{L_b,1}(t) = -C_b\frac{dv_{C_b,1}(t)}{dt}$ and $i_{L_t,2}(t) = C_b\frac{dv_{C_b,2}(t)}{dt}$, which enable the calculation of peak currents in the input inductors. Varying duty ratios lead to different current distributions between the two input inductors. For instance, when $D = \frac{1}{3}$, a greater portion of current flows into L_b, resulting in more energy being stored in the bottom inductor than the top inductor, assuming equal inductance for both inductors. To reduce peak energy storage, the inductance of L_b can initially be decreased; however, beyond a certain point, the resulting increase in peak current of L_b may offset this benefit, potentially leading to a rise in overall energy storage. As such, an optimal value of L_b exists that minimizes the total volume. As illustrated in Fig 11(a), with the testbed configuration where $L_t = L_b$, L_t is held constant while L_b is swept until the minimum total volume is reached. The minimum occurs when L_b is reduced by approximately 0.81 order of magnitude. Similarly, as illustrated in Fig. 11(b), when $D = \frac{2}{3}$, more current flows into L_t. Therefore, L_b is held constant while L_t is varied to minimize the volume. In this configuration, reducing L_t by approximately 1.12 orders of magnitude minimizes the total volume of the passive components. Fig. 11(c) shows the influence of the bypass capacitance on the switch stress, which provides insights into optimal switch selection for designers.

V. Conclusion

This paper presents a comprehensive analysis of the input inductor buck converter, which is applicable across various operating conditions and component parameters. The proposed model enables designers to determine optimal passive component values based on specific requirements under diverse



(a) (b) (c)

Fig. 11: Passive component values analysis when $V_{in} = 48$ V, $R = 5\ \Omega$, $f_{sw} = 521.72$ kHz and $\rho_{E,L} = 10\ \mu$J/cm^3. (a) Total volume of passive components versus inductance of the bottom inductor, where $D = \frac{1}{3}$, $L_t = 33\ \mu$H and $C_b = 0.282\ \mu$F. (b) Total volume of passive components versus inductance of the top inductor, where $D = \frac{2}{3}$, $L_b = 33\ \mu$H and $C_b = 0.282\ \mu$F. (c) Peak switch stress versus capacitance of the bypass capacitor, where $D = \frac{1}{2}$, and $L_t = L_b = 33\ \mu$H.

operating conditions. Furthermore, this work establishes a solid foundation for analyzing other topologies with split inductors, extending its applicability to future tolologies.

REFERENCES

[1] K. Radhakrishnan, M. Swaminathan, and B. K. Bhattacharyya, "Power delivery for high-performance microprocessors—challenges, solutions, and future trends," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 4, 2021, pp. 655–671.

[2] K. Wang, S. Y. Sim, Y. Q. Choong, S. Pakala, X. Zhang, and C. Huang, "A high density three-level quadratic buck hybrid converter for 48v-to-pol conversion," in *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2025.

[3] A. K. Delmar and A. Stillwell, "Current-sourced hybrid switched-capacitor converter for data center power delivery," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 1357–1362.

[4] W. W. Weaver and P. T. K. Krein, "Analysis and applications of a current-sourced buck converter," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 2007, pp. 1664–1670.

[5] M. Karppanen, J. Arminen, T. Suntio, K. Savela, and J. Simola, "Dynamical modeling and characterization of peak-current-controlled superbuck converter," in *IEEE Transactions on Power Electronics*, vol. 23, no. 3, 2008, pp. 1370–1380.

[6] R. S. Bayliss and R. C. Pilawa-Podgurski, "An input inductor flying capacitor multilevel converter utilizing a combined power factor correcting and active voltage balancing control technique for buck-type ac/dc grid-tied applications," in *2024 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2024, pp. 1–7.

[7] S. Coday, D. Menzi, J. Huber, and J. W. Kolar, "A novel non-mirrored buck-boost flying capacitor multilevel dc-dc converter topology," in *2022 IEEE 7th Southern Power Electronics Conference (SPEC)*, 2022, pp. 1–6.

[8] N. C. Brooks, J. Zou, S. Coday, T. Ge, N. M. Ellis, and R. C. N. Pilawa-Podgurski, "On the size and weight of passive components:scaling trends for high-density power converter designs," in *IEEE Transactions on Power Electronics*, vol. 39, no. 7, 2024, pp. 8459–8477.

[9] C. R. Sullivan, B. A. Reese, A. L. F. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1–23.