

The Design and Analysis of a Capacitively-Isolated Series-Parallel Converter

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Abstract—Series-input, parallel-output power converters are an effective solution for applications requiring high power density and large conversion ratios. Hybrid switched-capacitor topologies are a compelling alternative to the traditional magnetics-based topologies commonly used in stacked converters. One required feature of these series-input, parallel-output converters is the ability to achieve electrical isolation between the input and output grounds. Capacitor-based isolation enables low passive volume, indicating the potential for use in weight- and volume-constrained application spaces. This work presents a capacitively-isolated variant of the series-parallel hybrid switched-capacitor converter capable of at- and above-resonance operation. Analysis and operation for symmetric and asymmetric variants of the capacitively-isolated series-parallel converters are presented. The converters presented in this work are compared to existing capacitively-isolated hybrid switched-capacitor converters via passive volume and switch stress analysis. Experimental results of a prototype of the 4:1 capacitively-isolated series-parallel converter validate the analysis.

Index Terms—hybrid switched-capacitor converter, series-parallel converter capacitively-isolated converter

I. INTRODUCTION

Typical solutions for applications requiring extreme conversion ratios, such as those in data center computing, aircraft power delivery, or tethered robots in space, experience challenges associated with high current and voltage stresses across devices [1]–[3]. One approach that mitigates these challenges while enabling high energy density and output regulation is the composite converter. Such series-input, parallel-output converters are often realized as stacked LLC modules or other transformer based converters [4]. However, magnetics-based topologies experience limitations due to the scaling of magnetics [5]. Hybrid switched-capacitor power converters (HySC) can be competitive with conventional magnetics-based converters in both efficiency and passive component volume due to the utilization of energy dense capacitors as the primary medium of power transfer. Hybrid switched-capacitor converters also enable lower stress across the switching devices, which is a desirable converter characteristic due to improved figures of merit for lower voltage rated devices. Previous work has demonstrated the successful implementation of capacitive isolation in HySC topologies, specifically in the Dickson [6] and the Cockcroft-Walton [7] converters. For capacitive isolation, the dielectric material of the capacitors realizes the isolation barrier between the converter's input and output ground [8], [9]. While there are concerns that

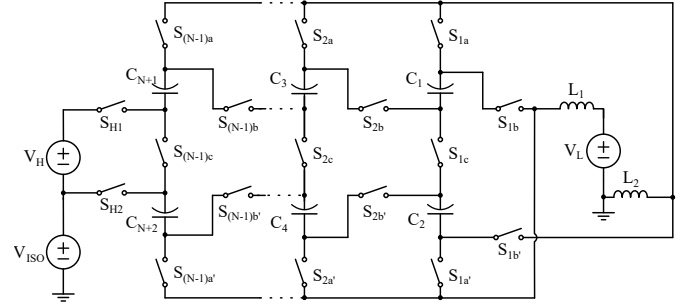


Fig. 1. The generalized symmetric capacitively-isolated SP converter.

capacitive isolation cannot yet meet the standards required for safety rated isolation, capacitors as an isolation method are a strong candidate for use in composite converters, which require isolation in all but the ground-referenced converter. Therefore, this work investigates the introduction of capacitive isolation barriers into additional HySC converters for applications in stacked converters. Previous capacitively-isolated HySC converters were restricted to at-resonance operation. This work presents a capacitively-isolated variant of the series-parallel (SP) converter that is able to operate at- and above-resonance. Above-resonance operation reduces the ripple and root mean squared (RMS) current on the inductors, leading to an overall reduction in inductor stress. However, with above-resonance operation zero current switching (ZCS) is lost, which increases switching losses. This work provides a preliminary generalized analysis of the topology and shares the design and characterization of a 4:1 hardware prototype converter.

II. SYMMETRIC CAPACITIVELY-ISOLATED SERIES-PARALLEL CONVERTER

A. Resonant Frequency

The symmetric capacitively-isolated SP converter is shown in Fig. 1. The resonant frequencies of the converter are shown for phase one, f_1 , and phase two, f_2 , in (1) when $C_0 = C_1 = C_2 = \dots = C_{N+2}$ and $L_0 = L_1 = L_2$. Figure 2 shows the two phase operation of the symmetric capacitively-isolated SP converter at $N = 4$. Using charge flow as in [10], it is determined that each capacitor discharges or charges by

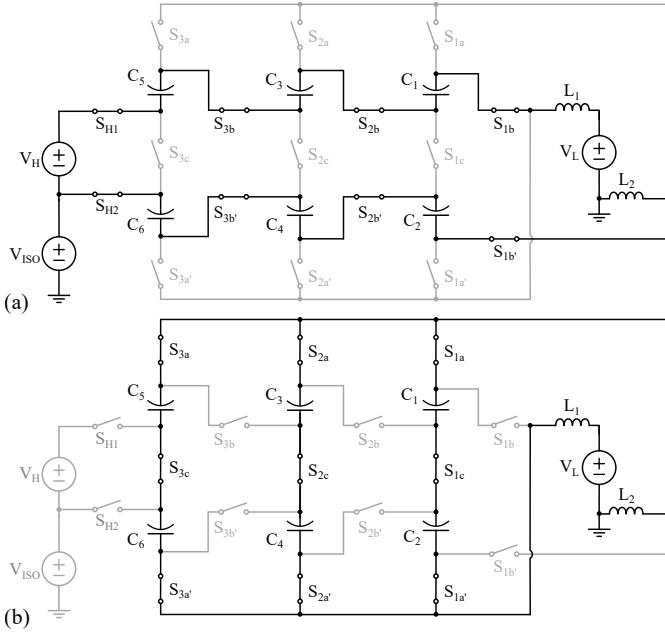


Fig. 2. Two-phase operation of the 4:1 converter for phases (a) one and (b) two.

an equal amount, q . As such, equal capacitance was chosen to maintain equal voltage ripple on the capacitors.

$$\begin{aligned} f_1 &= \frac{1}{2\pi} \sqrt{\frac{N-1}{L_0 C_0}} \\ f_2 &= \frac{1}{2\pi} \sqrt{\frac{1}{L_0 C_0 (N-1)}} \end{aligned} \quad (1)$$

B. Phase Timings

The resonant period, for a given period j , is defined as T_j for a given angular frequency, ω_j . Assuming the inductor current is half-wave resonant, as shown in Fig. 3a, the phase duration, t_j , is half the resonant period as seen in (2).

$$t_j = \frac{T_j}{2} = \frac{\pi}{\omega_j} \quad (2)$$

The phase normalization parameter, τ_j , relates the phase durations to the period of operation as in (3).

$$\tau_j = \frac{t_j}{\sum_i t_i} = \frac{t_j}{T} \quad (3)$$

For the symmetric capacitively-isolated SP converter with two phase operation, the phase normalization vector, τ , is shown in Table I. The summation of phase durations is equal to the period of operation, T . For the symmetric capacitively-isolated SP converter, the period of operation, T_{symm} , is the summation of t_1 and t_2 and expressed in (4).

$$T_{\text{symm}} = \pi \sqrt{L_0 C_0 \left(\frac{1}{N-1} + \frac{N-1}{1} \right)} \quad (4)$$

The time durations and operation period for the symmetric capacitively-isolated SP converter exactly match those of the non-isolated SP converter [11].

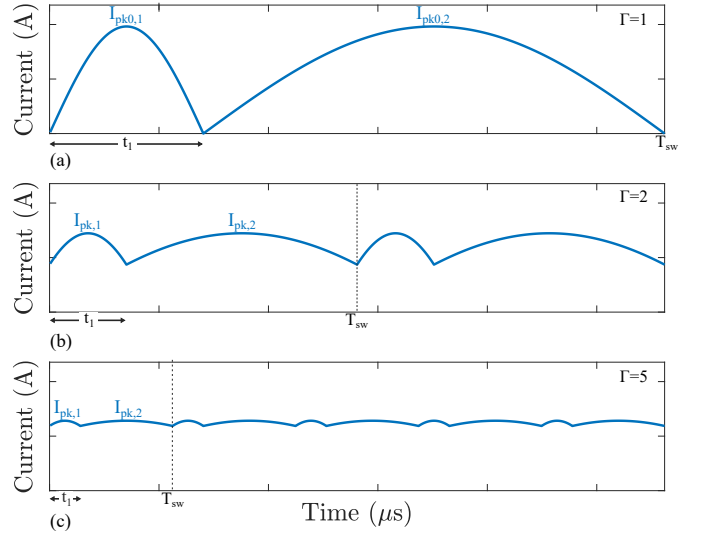


Fig. 3. Inductor currents for SP converters operated at various values of Γ .

C. Inductor Current

The at-resonance inductor current can be determined using the methods presented in [11]. The generalized form of inductor current expressed in terms of the dc output current I_{out} is presented in (5).

$$i_{L,j}(t) = \frac{\pi}{2} I_{\text{out}} \sin(\omega_j t) \quad (5)$$

D. Capacitor Voltages

Initial analysis of capacitor voltages results in under-constrained mid-range voltages. Each capacitor's voltage can be expressed as in (6), where α_n and β_n are unknown scaling factors. This work does not include the derivation of α_n and β_n , but will present experimentally derived values for these scaling factors. Notably, at $|\beta_{N+2}| = |\beta_{N+1}| = 1$ the switch voltages are independent of isolation voltage.

$$V_{C_n} = \alpha_n V_H + \beta_n V_{\text{ISO}} \quad (6)$$

The capacitor voltage vector v_c of Table I were derived using the assumptions that $\alpha_1 = \alpha_2 = \dots = \alpha_N = \frac{1}{2N}$ and $\beta_1 = \beta_2 = \dots = \beta_N = 0$. The experimental results presented in Section VI will validate these assumptions.

E. Above-Resonance Operation

The inductors L_1 and L_2 are located at the output, as a result, the converter can be operated both at- and above-resonance. For above-resonance operation, the switch frequency is the resonant frequency multiplied by a scaling factor, Γ , defined in (7).

$$\Gamma = \frac{f_{\text{sw}}}{f_{\text{res}}} \quad (7)$$

The phase timings of (2) can then be expressed as a function of Γ as in (8). For this converter, the phase normalization vector is unchanged.

$$t_j = \frac{T_j}{2\Gamma} = \frac{\pi}{\omega_j \Gamma} \quad (8)$$

At $\Gamma = 1$, the inductor current can be defined as in (9), where $I_{pk0,j}$ is the peak of the inductor current waveform at-resonance as shown in Fig. 3. The phase shift $\theta_{0,j}$ is the relative phase shift between phases j and $j + 1$ necessary to ensure continuity of current.

$$i_{L,j|\Gamma=1}(t) = I_{pk0,j} \sin(\omega_j t + \theta_{0,j}) \quad (9)$$

As Γ increases above one, the minimum inductor current value increases, the maximum inductor current value decreases, and the average inductor current value remains the same and equal to the output current. This results in the convergence of the inductor current to the output current as $\Gamma \rightarrow \infty$. To determine an equation for inductor current as Γ increases above one, a phase shift, θ_j , and dc offset, $I_{v,j}$ can be applied to the inductor current at $\Gamma = 1$. Thus, the above resonance inductor current can be expressed as in (10).

$$i_{L,j}(t) = I_{pk0,j} \sin(\omega_j t + \theta_j) + I_{v,j} \quad (10)$$

Figure 4 demonstrates the steps necessary to determine the inductor current above-resonance. In Fig. 3a, the $\Gamma = 1$ inductor current is shown. The equations representing the inductor current in this figure are a piecewise function expressed in (11) in terms of (9). While Fig. 3 shows two phase operation, this analysis can be applied to multi-phase operation.

$$i_L(t) = \begin{cases} i_{L,1|\Gamma=1}(t) & \text{for } 0 < t < t_1 \\ i_{L,2|\Gamma=1}(t) & \text{for } t_1 < t < T_{sw} \end{cases} \quad (11)$$

As an example, moving from $\Gamma = 1$ to $\Gamma = 2$, the period is reduced by a factor of two. As such, the time durations, t_j , of each phase decrease by a factor of two. The half-wave resonant inductor current equation that satisfies these timing requirements is depicted by i_a in Fig. 4a. To simplify the inductor current analysis, i_a is phase shifted such that it can be expressed as i_b in (12).

$$i_b(t) = \begin{cases} i_a(t + \frac{\theta_1}{\omega_1}) & \text{for } 0 < t < \frac{t_1}{2} \\ i_a(t + \frac{\theta_2}{\omega_2}) & \text{for } \frac{t_1}{2} < t < T_{sw} \end{cases} \quad (12)$$

The phase shift is achieved by taking the difference of the at-resonance and above-resonance phase durations while a factor of $\frac{1}{2}$ maintains the symmetry of the sinusoid. An expression for θ_1 is presented in (13).

$$\begin{aligned} \theta_1 &= \omega_1 \left(\frac{t_{1|\Gamma=1}}{2} - \frac{t_{1|\Gamma}}{2} \right) \\ &= \frac{\pi}{2} - \frac{\pi}{2\Gamma} \end{aligned} \quad (13)$$

The average inductor current should be equal across all values of Γ , but the average value of i_b , shown in Fig. 4b as a dashed orange line, is greater than average inductor current at $\Gamma = 1$ which is shown in Fig. 4b as a dashed black line. The difference between the average output current and the average of i_b , labeled in Fig. 4b, is the vertical offset, I_v . A generalized equation for $I_{v,j}$ in terms of the average inductor

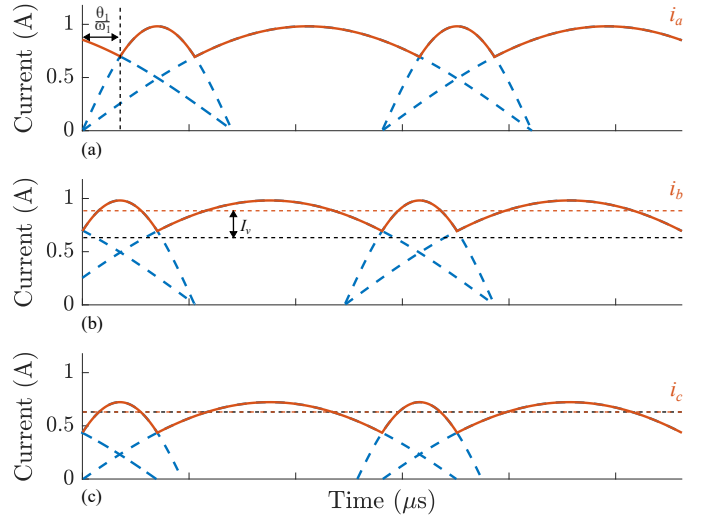


Fig. 4. Inductor current for operation above-resonance depicting necessary transformations to maintain a fixed dc output current at- and above-resonance. The orange curves represent the $\Gamma = 2$ waveforms.

current at $\Gamma = 1$ and the average of the inductor current waveform without the vertical offset applied is shown in (14).

$$I_{v,j} = I_{L,j|\Gamma=1} - \frac{1}{t_j} \int_{t_{j-1}}^{t_{j-1}+t_j} I_{pk0,j} \sin(\omega_j t + \theta_j) dt \quad (14)$$

In Fig. 4c, i_c shows the final inductor current with the phase and vertical offsets applied. This inductor current is equal to that of Fig. 3b. Using (10) the average inductor current can be expressed as in (15).

$$I_{L,j} = \frac{1}{t_j} \int_{t_{j-1}}^{t_{j-1}+t_j} I_{pk0,j} \sin(\omega_j t + \theta_j) + I_{v,j} dt \quad (15)$$

The average output current can then be expressed as in (16).

$$I_{out} = \frac{\Gamma}{T} \sum_j \left(\int_{t_{j-1}}^{t_{j-1}+t_j} i_j(t) dt \right) \quad (16)$$

The per phase inductor charge can be determined through charge flow [10]. The normalized inductor charge flow matrix, a_L , relates the per phase inductor charge to q_{HI} . The charge through the inductor in phase j can be expressed as the integral of the inductor current (17).

$$\begin{aligned} q_j &= \int_{t_{j-1}}^{t_{j-1}+t_j} I_{pk0,j} \sin(\omega_j t + \theta_j) + I_{v,j} dt \\ &= \frac{2I_{pk0,j}}{\omega_j} \cos(\omega_j t_{j-1} + \theta_j) + I_{v,j} \left(\frac{\pi}{\omega_j \Gamma} \right) \end{aligned} \quad (17)$$

Evaluating the integral of (17) results in an equation for $I_{pk0,j}$, the amplitude of at-resonance inductor current, in terms of the inductor charge flow and angular frequency of the phase (18).

$$\begin{aligned} I_{pk0,j} &= \frac{q_j \omega_j - I_{v,j} \left(\frac{\pi}{\Gamma} \right)}{2 \cos(\omega_j t_{j-1} + \theta_j)} \\ &= \frac{q_{HI} a_{L,j} \omega_j - I_{v,j} \left(\frac{\pi}{\Gamma} \right)}{2 \cos(\omega_j t_{j-1} + \theta_j)} \end{aligned} \quad (18)$$

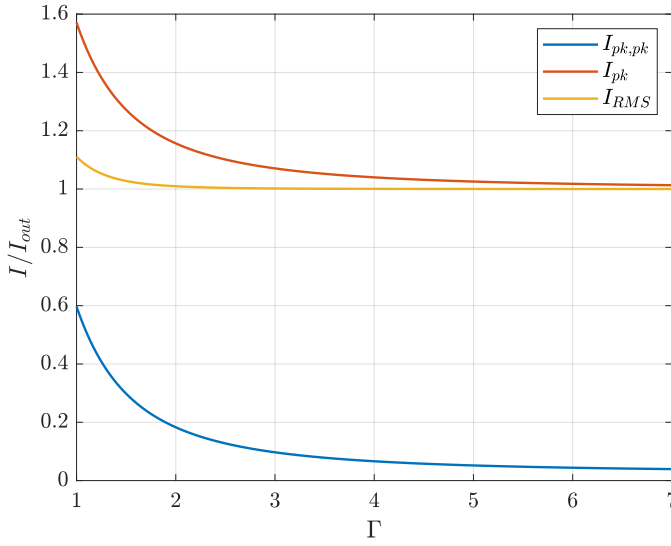


Fig. 5. Relevant component sizing parameters, $I_{pk,pk}$, I_{pk} , and I_{RMS} normalized to I_{out} as a function of Γ .

Current continuity between phases provides another expression for $I_{pk0,j}$ (19).

$$\begin{aligned} I_{pk0,j} \sin(\omega_j t_j + \theta_j) + I_{v,j} \\ = I_{pk0,j+1} \sin(\omega_{j+1} t_j + \theta_{j+1}) + I_{v,j+1} \end{aligned} \quad (19)$$

As all topologies considered in this work operate in two phases, further analysis will assume two-phase operation for simplicity. Previous work shows a similar derivation for multiphase operation [11]. The average inductor current per phase is equal to the charge for each period divided by the respective period duration. The average current in each phase can therefore be expressed as shown in (20).

$$\frac{I_{L,1}}{I_{L,2}} = \frac{a_{L,1}\omega_1}{a_{L,2}\omega_2} \quad (20)$$

The right hand side of the equation can be evaluated using Table I for all topologies presented here. Note that for the symmetric SP converters, $\frac{a_{L,1}\omega_1}{a_{L,2}\omega_2} = 1$. Thus, the average currents and consequently the vertical offsets, $I_{v,1}$ and $I_{v,2}$, are equal. With $I_{v,1} = I_{v,2} = I_v$, (18) and (19) can be simplified to express the ratio of $I_{pk0,1}$ to $I_{pk0,2}$ as seen in (21)

$$\begin{aligned} \frac{I_{pk0,1}}{I_{pk0,2}} &= \frac{\cos(\frac{\omega_2}{\omega_1} \frac{\pi}{\Gamma} + \theta_2)}{\cos(\theta_1)} \\ &= \frac{\sin(\frac{\omega_2}{\omega_1} \frac{\pi}{\Gamma} + \theta_2)}{\sin(\frac{\pi}{\Gamma} + \theta_1)} \end{aligned} \quad (21)$$

Since the inductor current in each phase starts and ends at the same value and the waveform is half-wave symmetric, the identities presented in (22) may be used.

$$\begin{aligned} \sin(\theta_1) &= \sin(\frac{\pi}{\Gamma} + \theta_1) \\ \cos(\theta_1) &= -\cos(\frac{\pi}{\Gamma} + \theta_1) \end{aligned} \quad (22)$$

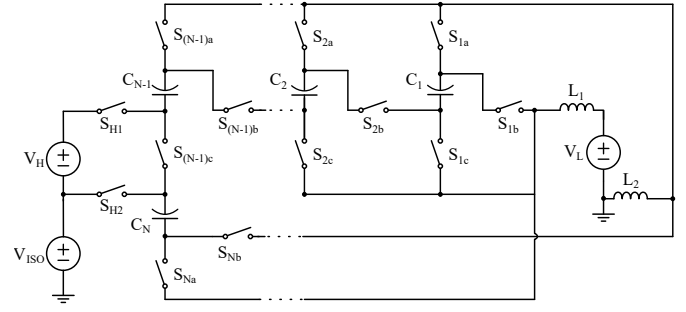


Fig. 6. The generalized asymmetric converter variant. In phase one, the switches labeled with a b or H are on. In phase two, the switches labeled with an a or c are on.

Therefore, using (22), (21) can be solved for the relationship between θ_1 and θ_2 expressed in (23).

$$\theta_1 = \theta_2 + \frac{\omega_2}{\omega_1} \frac{\pi}{\Gamma} \quad (23)$$

Equations (21), (22), and (23) show that the peak inductor currents are equal: $I_{pk0,1} = I_{pk0,2} = I_{pk0}$. As I_{pk0} is not a function of Γ , it can be solved using resonance conditions of $\Gamma = 1$ and $I_v = 0$. I_{pk0} as a function of I_{out} is shown in (24).

$$I_{pk0} = \frac{\pi}{2} I_{out} \quad (24)$$

I_v , in terms of I_{out} and Γ , can be determined from (14). The resultant equation is expressed in (25).

$$I_v = \left(1 - \Gamma \cos\left(\frac{\pi(\Gamma-1)}{2\Gamma}\right) \right) I_{out} \quad (25)$$

Expressions for inductor currents $i_{L,1}$ and $i_{L,2}$ in terms of I_{out} and as a function of Γ are shown in (26) and (27), respectively.

$$\begin{aligned} i_{L,1}(t) &= \frac{\pi}{2} I_{out} \sin\left(\omega_1 t + \frac{\pi(\Gamma-1)}{2\Gamma}\right) \\ &+ \left(1 - \Gamma \cos\left(\frac{\pi(\Gamma-1)}{2\Gamma}\right) \right) I_{out} \end{aligned} \quad (26)$$

$$\begin{aligned} i_{L,2}(t) &= \frac{\pi}{2} I_{out} \sin\left(\omega_2 t + \frac{\pi(\Gamma-1)}{2\Gamma} - \frac{\omega_2 \pi}{\omega_1 \Gamma}\right) \\ &+ \left(1 - \Gamma \cos\left(\frac{\pi(\Gamma-1)}{2\Gamma}\right) \right) I_{out} \end{aligned} \quad (27)$$

The normalized inductor peak current, I_{pk} , peak to trough current, $I_{pk,pk}$, and RMS current are plotted as a function of Γ in Fig. 5. At $\Gamma < 2$, the inductor $I_{pk,pk}$, I_{pk} , and I_{RMS} decrease rapidly while at values $\Gamma > 2$ the rate of decline decreases and eventually plateaus. While increasing Γ provides component stress and sizing benefits, due to the reduction in these currents, there are marginal benefits to increasing Γ to values larger than two. Furthermore, increasing Γ proves disadvantageous as it leads to increased switching losses. Thus, Fig. 5 motivates limiting above-resonance operation to less than twice the resonant frequency.

III. ASYMMETRIC CAPACITIVELY-ISOLATED SERIES-PARALLEL CONVERTER

The capacitively-isolated SP converter can also be implemented asymmetrically as in Fig. 6. The asymmetric variant of the converter has reduced component count compared to the symmetric variant as detailed in Table I.

A. Resonant Frequency

The resonant tanks of the asymmetric capacitively-isolated SP converter are expressed in (28) with $C_0 = C_1 = C_2 = \dots = C_{N-2}$ and $2C_0 = C_{N-1} = C_N$. The inductor values are imbalanced with $L_0 = L_1$, and $L_2 = \frac{L_0}{2^{N-3}}$. This capacitance relationship was chosen such that the parallel branches of phase two have equal effective capacitance. The inductor relationship was chosen for equal resonance between the LC tanks of phase one.

$$\begin{aligned} f_1 &= \frac{1}{2\pi} \sqrt{\frac{2N-3}{2L_0C_0}} \\ f_2 &= \frac{1}{2\pi} \sqrt{\frac{2N-3}{2(N-1)^2L_0C_0}} \end{aligned} \quad (28)$$

B. Phase Timings

The phase normalization vector, τ , is expressed in Table I. The phase normalization vectors, and consequently the phase timings, for the two variants of the capacitively-isolated SP converter are the same. The period of operation for the asymmetric capacitively-isolated SP converter equals that of the symmetric variant and is expressed in (29).

$$T_{asym} = \pi \sqrt{2L_0C_0 \left(\frac{1}{2N-3} + \frac{(N-1)^2}{2N-3} \right)} \quad (29)$$

C. Inductor Current

For the asymmetric capacitively-isolated SP converter, the inductor currents can be calculated using the method presented for the symmetric capacitively-isolated SP converter shown in Section II-C. The symmetric and asymmetric capacitively-isolated SP converters have the same normalized charge flow matrix, a_L , and the same ratio of resonant frequencies, $\frac{f_1}{f_2}$. Due to these similarities, the inductor current analysis for the symmetric capacitively-isolated SP converter holds for the asymmetric capacitively-isolated SP converter.

D. Capacitor Voltages

The mid-range voltages experienced by the capacitors are shown in Table I.

IV. PASSIVE COMPONENT SIZING

A comparison of capacitively-isolated converter topologies via passive component sizing was conducted according to the analytical method presented in [11], in which the total passive volume of a converter is determined by relating the peak energy stored in each passive component to the volume using a volumetric energy density factor. Previous work developed generalized equations for capacitor volume in terms of the vectors of Table I. For the inductor volume, the peak energy

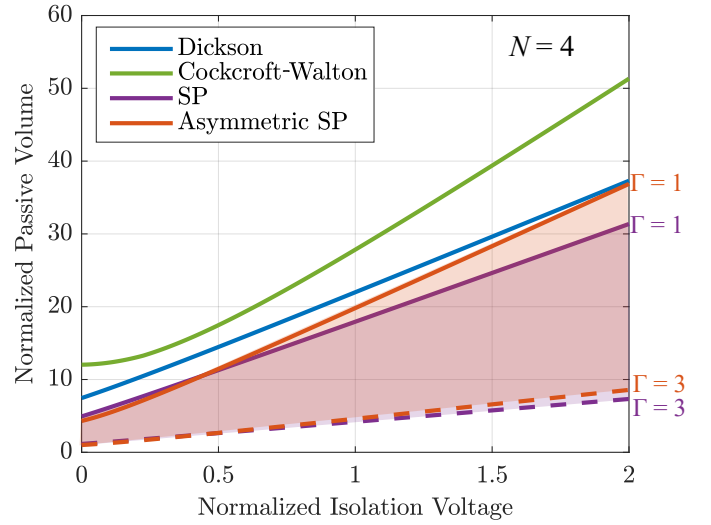


Fig. 7. Normalized isolation voltage versus normalized passive volume of capacitively-isolated HySC topologies operating at- and above-resonance.

stored in the inductors was calculated using the inductor current derivation of Section II-E as shown in (30). The maximum peak energy stored in the inductors was then converted to a volume using the volumetric energy density.

$$\begin{aligned} E_{L,pk_j} &= \frac{1}{2} L_j I_{pk,j}^2 \\ &= \frac{q_{HI}}{2C_0\kappa_j} \left(\frac{N\tau_j}{\pi} \left(\frac{\pi}{2} + 1 - \Gamma \cos \theta_j \right) \right)^2 \end{aligned} \quad (30)$$

Using Table I, the characteristic vectors for the symmetric and asymmetric variants of the capacitively-isolated SP converter were determined for $N = 4$. The capacitively-isolated Dickson converter and capacitively-isolated Cockcroft-Walton converter were analyzed at resonant operation. The capacitively-isolated Cockcroft-Walton converter was analyzed with distributed inductance to maintain soft-charging on the capacitors across all topologies compared [7]. The symmetric and asymmetric variants of the capacitively-isolated SP converter were analyzed at- and above-resonance. Figure 7 plots the normalized passive volume of each converter against isolation voltage normalized to the high side voltage, e.g. $\frac{V_{ISO}}{V_H}$. For normalized isolation voltages less than two, both capacitively-isolated SP converters have lower normalized passive volume than the Dickson and Cockcroft-Walton converters. Increasing Γ reduces the peak inductor current as shown in Fig. 5, as such above-resonance operation results in a decrease in normalized passive volume. Furthermore, above-resonance operation reduces the sensitivity to component mismatch. Thus, the use of Class 2 multilayer ceramic capacitors (MLCC), which have higher energy density than Class 1 MLCCs, could further reduce the passive volume of the components presented in Fig. 7 [12].

TABLE I
CHARACTERISTIC VECTORS FOR CAPACITIVELY-ISOLATED HYBRID SWITCHED CAPACITOR CONVERTERS

Topology	Symmetric Series-parallel $N \in \{N \geq 2\}$	Asymmetric Series-Parallel $N \in \{N \geq 2\}$
N_p	2	2
N_c	$2(N-1)$	N
N_s	$5N-3$	$3N+1$
N_{sa}	$2(N-1)$	N
N_{sb}	$2(N-1)$	N
N_{sc}	$N-1$	$N-1$
N_{sh}	2	2
$a_{c[N_p \times N_c]}$	$\begin{bmatrix} 1 & 1 & \dots & 1 \\ -1 & -1 & \dots & -1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & \dots & 1 \\ -1 & -1 & \dots & -1 \end{bmatrix}$
$a_{L[N_p \times 2]}$	$\begin{bmatrix} 1 & 1 \\ N-1 & N-1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 \\ N-1 & N-1 \end{bmatrix}$
$v_{c[1 \times N_c]}$	$\begin{bmatrix} \frac{1}{2N} & \dots & \frac{1}{2N} & \frac{3}{2N} + \frac{V_{iso}}{V_H} & -\frac{V_{iso}}{V_H} - \frac{1}{N} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N} & \dots & \frac{1}{N} & \frac{1}{N} + \frac{V_{iso}}{V_H} & -\frac{V_{iso}}{V_H} \end{bmatrix}$
$c[1 \times N_c]$	$\begin{bmatrix} 1 & 1 & \dots & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & \dots & 1 & 2 & 2 \end{bmatrix}$
$l[1 \times 2]$	$\begin{bmatrix} 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & \frac{1}{2N-3} \end{bmatrix}$
$v_{sa[1 \times \frac{N_{sa}}{2}]}$	$\begin{bmatrix} \frac{2}{2N} & \frac{3}{2N} & \dots & \frac{N}{2N} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N} & \frac{2}{N} & \dots & \frac{N-1}{N} & \frac{1}{N} \end{bmatrix}$
$v_{sb[1 \times \frac{N_{sb}}{2}]}$	$\begin{bmatrix} \frac{1}{N} & \frac{1}{2N} & \frac{1}{2N} & \dots & \frac{1}{2N} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N} & \frac{1}{N} & \dots & \frac{1}{N} \end{bmatrix}$
$v_{sc[1 \times N_{sc}]}$	$\begin{bmatrix} \frac{2}{N} & \frac{3}{N} & \dots & \frac{N-1}{N} & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N} & \frac{2}{N} & \dots & \frac{N-1}{N} & 1 \end{bmatrix}$
$v_{sh[1 \times 2]}$	$\begin{bmatrix} \frac{2N-1}{2N} & \frac{1}{2N} \end{bmatrix}$	$\begin{bmatrix} \frac{N-1}{N} & \frac{1}{N} \end{bmatrix}$
$\kappa[N_p \times 1]$	$\begin{bmatrix} 1 \\ N-1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{2N-3} \\ \frac{2(N-1)^2}{2N-3} \end{bmatrix}$
$\tau[N_p \times 1]$	$\begin{bmatrix} \frac{1}{N-1} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N-1} \end{bmatrix}$

V. SWITCH STRESS

Switch stress is calculated as in (31) where V_{ds} is the drain-to-source voltage of the switch assuming zero voltage ripple.

$$M_s = \frac{\sum_{switches} V_{ds} I_{ds,RMS}}{V_H I_H} \quad (31)$$

A. Symmetric Capacitively-Isolated Series-Parallel Converter

1) *Switch Currents*: The switch currents can be expressed in terms of the inductor currents derived in Sections II-C and II-E. Using charge flow as in [10], it is determined that each capacitor discharges or charges by an equal amount, q . Thus, the capacitor currents are of equal magnitude. In phase two, there are $N-1$ parallel combinations of capacitors. As such the phase two switch currents are $\frac{i_{L,2}}{N-1}$. The generalized switch currents are shown in (32).

$$I_{ds,l} = \begin{cases} i_{L,1} & \text{for } l = [kb, kb', H1, H2] \\ \frac{i_{L,2}}{N-1} & \text{for } l = [ka, ka', kc] \end{cases} \quad (32)$$

The RMS value of the inductor current is expressed in (33).

$$I_{j,RMS} = \left[I_{pk0}^2 \left(\frac{\Gamma}{2\pi} \sin\left(\frac{\pi}{\Gamma}\right) + \frac{1}{2} \right) - \frac{4\Gamma I_{pk0} I_v}{\pi} \cos\left(\frac{\pi(\Gamma-1)}{2\Gamma}\right) + I_v^2 \right]^{\frac{1}{2}} \quad (33)$$

2) *Switch Voltages*: With the same assumptions presented in Section II-D yields the generalized switch voltages presented in Table I. The switch voltages for the complimentary pairs of switches (a, a') and (b, b') are the same. While the zero voltage ripple assumption holds for the perfectly matched

capacitively-isolated Dickson converter and the Cockcroft-Walton with distributed inductance, it results in an under-estimate in switch stress for the capacitively-isolated symmetric and asymmetric SP converters.

B. Asymmetric Capacitively-Isolated Series-Parallel Converter

1) *Switch Currents*: As in the symmetric variant of the converter, the switch on-state currents can be expressed in terms of the inductor currents. Using charge flow [10], it is determined that the on-state currents of the phase two switches are $\frac{i_{L,2}}{N-1}$. The generalized switch currents for the asymmetric SP converter are shown in (34).

$$I_{ds,l} = \begin{cases} i_{L,1} & \text{for } l = [kb, H1, H2] \\ \frac{i_{L,2}}{N-1} & \text{for } l = [ka, kc] \end{cases} \quad (34)$$

2) *Switch Voltages*: The generalized switch voltages for the asymmetric capacitively-isolated SP converter, under a zero voltage ripple assumption, are expressed in Table I.

The at-resonance switch stress of the capacitively-isolated Dickson, Cockcroft-Walton, symmetric SP, and asymmetric SP converters are presented in Fig. 8. Above-resonance switch stress is presented for the capacitively-isolated symmetric and asymmetric SP converters. The Dickson and Cockcroft-Walton converters achieve significantly lower switch stress compared to the symmetric and asymmetric SP converters. While operating the SP converter variants above-resonance reduces their overall switch stress, the Dickson and Cockcroft-Walton converters still have reduced switch stress.

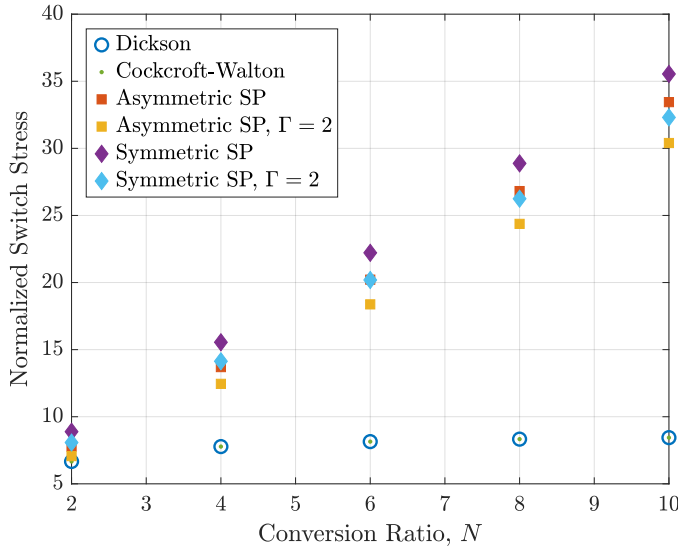


Fig. 8. Conversion ratio, N , versus normalized switch stress of capacitively-isolated HySC topologies operating at- and above-resonance.

VI. HARDWARE DESIGN AND RESULTS

A 4:1 capacitively-isolated SP converter prototype was built to validate the proposed topology, shown in Fig. 11 with components listed in Table II. The prototype board uses a dual sided design which separates the switching cells from the power processing capacitors. Due to the high number of switching cells, care was taken to minimize the commutation loops within the cells as well as between contiguous switching devices. Signal and power isolation were achieved using ADUM5241s, though future implementations may employ bootstrapping methods to improve overall efficiency and to reduce board area. The experimental inductor current waveforms in Fig. 9 show operation of the converter at- and above-resonance. The alignment of the derived inductor currents (blue) and the measured inductor currents (orange) in Fig. 9 validates the inductor current analysis presented in Section II-E. Furthermore, the capacitor voltage waveforms in Fig. 7 show soft-charging of the capacitors. The capacitor voltages split experimentally such that isolation voltage is only on capacitors C_5 and C_6 ; consequently, the voltages on the remaining capacitors are independent of isolation voltages as seen in Fig. 7. The experimentally derived values of α_n and β_n are $\alpha_1 \approx \frac{1}{12}$, $\alpha_2 \approx \frac{2}{12}$, $\alpha_3 \approx \alpha_4 \approx \frac{1}{8}$, $\alpha_5 \approx \frac{1}{2}$, $\alpha_6 \approx -\frac{1}{4}$, $\beta_1 = \beta_2 = \beta_3 = \beta_4 = 0$, $\beta_5 = 1$, and $\beta_6 = -1$. The difference in α for $n < 4$ is likely due to imbalanced parasitics. Future work will investigate further the mechanisms and factors that experimentally determine α and β . The converter achieves a peak efficiency of 93.3%, not including gate drive losses, at $V_H = 100$ V with $I_{out} = 7.3$ A and $\Gamma = 1.2$. Under light load conditions, the efficiency decreases for all values of Γ seen in Fig. 11c. This indicates that under light load conditions the converter becomes switching loss dominated especially as Γ increases above one. At higher values of Γ , the converter was able to achieve higher power levels while

maintaining peak efficiency.

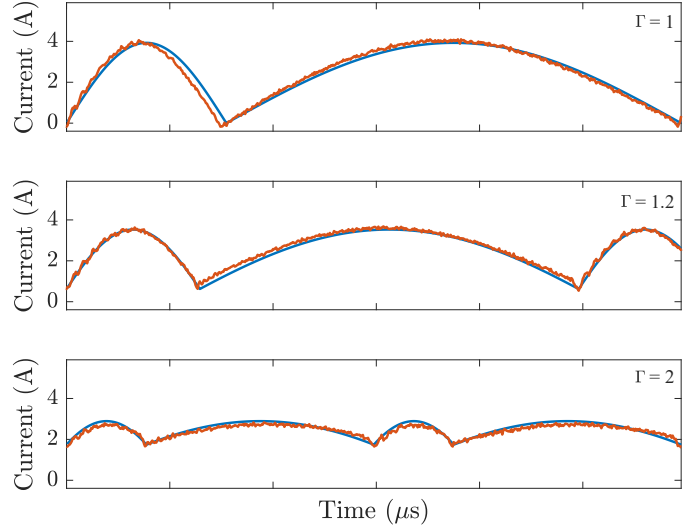


Fig. 9. Measured (orange) and calculated (blue) inductor current at $V_L = 12$ V, $V_{ISO} = 0$ V, $P_{out} \approx 130$ W, and $f_{sw} = 168$ kHz for (a) $\Gamma = 1$, (b) $\Gamma = 1.2$, and (c) $\Gamma = 2$.

Component	Part Number	Description
C_0	KEMET NP0	100 nF, 200 V
L_0	Würth 74438	600 nH, 3.2 mΩ
S	EPC 2034	200 V, 8 mΩ
Gate Driver	NCP81074	5 V, 10 A
Isolator	ADUM5241	Power and Signal

TABLE II
COMPONENTS FOR THE HARDWARE PROTOTYPE.

VII. CONCLUSION

This work has presented the analysis, design, and implementation of a 4:1 capacitively-isolated SP converter capable of operating at- and above-resonance and able to achieve capacitive isolation. Contributions include the resonant tank calculations and generalized inductor current equations for the symmetric and asymmetric variants of the capacitively-isolated SP converter. An initial hardware prototype of a 4:1 symmetric capacitively-isolated SP converter was presented, and the converter performance was verified at- and above-resonance with 0 V, 25 V, and 50 V of isolation. Finally, the inductor current analysis presented was validated both at- and above-resonance.

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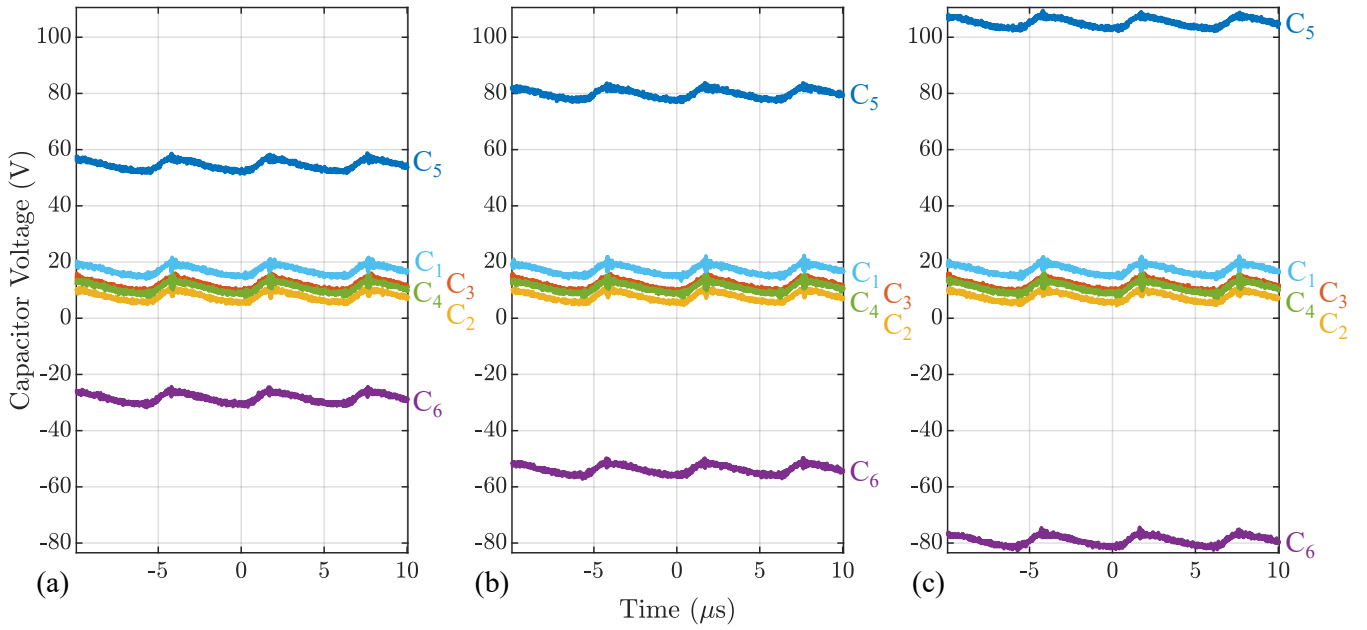


Fig. 10. Measured capacitor voltages with $V_H = 100$ V and an isolation voltage of (a) 0 V, (b) 25 V and (c) 50 V.

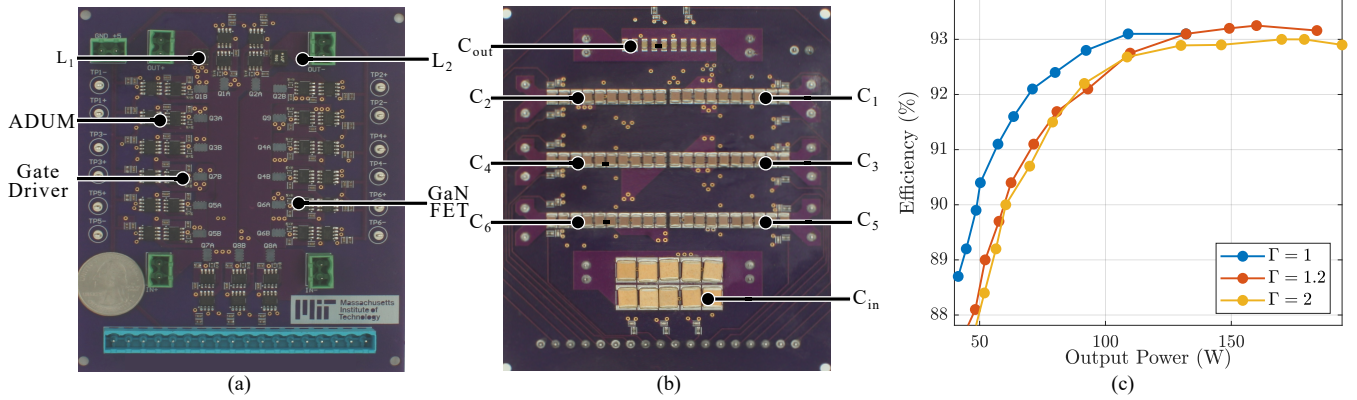


Fig. 11. Front (a) and back (b) sides of the hardware prototype of the 4:1 symmetric capacitively-isolated SP converter. An efficiency sweep (c) with $V_H = 100$ V for the converter is shown in (a) and (b).

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