The Design and Analysis of a Family of Capacitively-Isolated Hybrid Switched-Capacitor Converters

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***Abstract*—Series-input, parallel output converters can achieve extreme conversion ratios with high efficiency by utilizing a stacked architecture that relies on isolated converters. Typically, these isolated converters are magnetics-based modules. However, capacitive-based isolation is an emerging alternative to magnetics-based isolation particularly for volume- and weight-constrained applications as it provides reduced passive volume and eliminates the need for a ferrite core. Hybrid switched-capacitor converters are competitive with magnetics-based topologies as they achieve high energy density and reduced switch stresses. However, few capacitively isolated variants of hybrid switched-capacitor converters have been shown. This work presents a general framework for deriving capacitively isolated hybrid switched-capacitor converters from their non-isolated counterparts. Analysis and operation for three novel inductor-at-the-output topologies derived via this framework are presented. Through this framework, the derived topologies are compared to existing capacitively isolated hybrid switched-capacitor converters. Finally, experimental validation is provided for two of the presented topologies individually and in a 12:1 series-input, parallel output converter, validating operation principles and analysis.**

***Index Terms*—Hybrid switched-capacitor converter, multilevel converters, resonant converters, capacitive isolation, series-input parallel output**

I. Introduction

APPLICATIONS such as data center computing, more electric aircraft, and electric vehicle power delivery require advanced converters to achieve extreme conversion ratios, while maintaining high power density and efficiency. One approach is cascaded converters, a type of multi-stage converter architecture, in which the output of one converter is the input of the next converter. Consequently, the total gain is the product of each individual converters' gain. In these cascaded converter architectures, each stage processes the entire input power, which results in system efficiency lower than that of a single stage. A partial power processing converter architecture, the series-input, parallel-output (SIPO) converter architecture, mitigates these challenges while enabling high power density and maintaining high system efficiency because each converter processes a fraction of the input power. Unlike in cascaded converter architectures, isolated converters are required to realize a SIPO structure, as depicted in Fig. 1. Note that the converter connected to both input and output negative terminals, the bottom converter in Fig. 1, can be implemented as a non-isolated dc-dc converter, while the remaining converters must be isolated dc-dc converters. Typically, the converters are sized such that the isolated converters process most of the power [1]. While the isolated converters are often realized as LLC modules or other transformer-based converters [2], previous work has investigated capacitive isolation for SIPO converter architectures to achieve higher energy density [3], [4], [5], [6], [7]. Regardless of isolation method, these isolated dc-dc converters are able to achieve high efficiency at a fixed conversion ratio, resulting in high overall system efficiency. Previous implementations have shown that the non-isolated converter can be implemented as a regulating converter, which allows for a narrow range of regulation [1], [8].

Typical isolation methods utilize magnetic-based elements, such as transformers, which scale poorly to smaller sizes, inhibiting power-dense and efficient power conversion [9]. Due to the poor scaling of magnetic components, previous work has investigated alternate approaches to achieving isolation for power electronics. Piezoelectric components scale well and have been shown to achieve isolation [10], [11], [12]; however, piezoelectric-based isolation is currently limited by mounting of the piezoelectric component and load-dependent operation [13]. An alternative to magnetic- and piezoelectric-based isolation is capacitor-based isolation [14], [15], [16]. Capacitors scale favorably to smaller sizes, allowing for power-dense and efficient converters. Capacitive isolation has been investigated for various size and weight-constrained applications such as data center computing [17], [18], aircraft power delivery [16], and tethered robots in space [19].

The capacitive isolation strategies used in previous works are typically resonant tank based converters operated at resonance. Many of the strategies utilize two-level converters composed of an inverter, LC tank, and rectifier, which provide capacitive isolation with a fixed 1:1 conversion ratio [20],

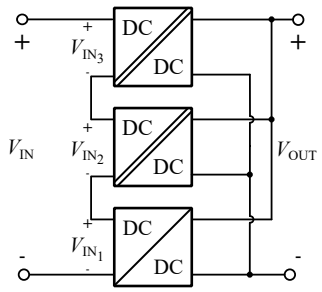


Fig. 1. A generalized implementation of a series-input, parallel-output partial power processing converter with two isolated converters and one non-isolated converter.

DOI: 10.1109/OJPEL.2026.3664036

[21]; however, control schemes such as phase shifted pulse width modulation allow for variable conversion ratios [7]. In addition, variants of this structure have been used to develop novel capacitively isolated topologies with both fixed and variable conversion ratios [22], [23]. Previous work utilizes topology derivation techniques such as duality [20], to derive capacitively isolated topologies from magnetics-based counterparts.

In non-isolated power conversion, multilevel converters provide reductions in component ratings providing increased power density and efficiency. Hybrid switched-capacitor converters, a family of multilevel capacitor-based non-isolated power converters, can be competitive with conventional magnetics-based converters in both efficiency and passive component volume due to the utilization of energy-dense capacitors as the primary medium of power processing [24]. While these benefits are seen in hybrid switched-capacitor converters operated at resonance, operation above resonance can further reduce the sizing of passive components, inductor ripple, and decrease sensitivity to frequency at the detriment of losing zero current switching (ZCS) [24], [25].

Recently, the use of capacitively isolated hybrid switched-capacitor converters, such as the Dickson [14], [26], Cockcroft-Walton [15], [27], and the flying capacitor multilevel (FCML) [18] converters, to provide isolation and a fixed conversion ratio has been investigated. In some of these variants, the isolation capacitors are solely used for isolation, while in others, they are also used for power processing. While maintaining the benefits of hybrid switched-capacitor converters in terms of passive component volume, efficiency, and reduced switch stress, these converters are limited to at-resonant operation, meaning they are sensitive to component mismatch and cannot benefit from above-resonant operation. Despite these benefits, hybrid switched-capacitor based capacitively isolated topologies may not out perform state-of-the-art magnetics-based isolation approaches; however, previous work indicates that capacitive isolation based SIPO converter architectures can provide lower loss and volume than magnetically isolated SIPO architectures [7]. As directly comparing capacitor- and magnetic-based isolation is difficult due to the challenges associated with modeling magnetic components' losses, this work focuses on providing a methodology for fundamentally comparing multilevel capacitively isolated converter topologies.

While introductory work has been done regarding capacitively isolated hybrid switched-capacitor converters for safety-rated isolation [18], [28], [23], such analysis is beyond the scope of this work. This work focuses on SIPO converter architectures where end-to-end system isolation is not necessary.

While the capacitively isolated series-parallel converter was previously presented by the authors [29], this work presents the derivation of this topology and extends it to other capacitively isolated converters. Thus, this work presents a systematic approach to introducing isolation in existing two-phase hybrid switched-capacitor converters while maintaining the ability to operate both at and above resonance. Novel capacitively isolated variants of the series-parallel [29], Fibonacci, and Dickson converters are presented and validated via experimental results. A method of comparing capacitively isolated hybrid switched-capacitor converters is derived using a method analogous to that presented in [30] but extended to capacitively isolated topologies.

This article is organized as follows: Section II presents a topological derivation framework for introducing isolation into existing hybrid switched-capacitor converters. Section III discusses the operation of the proposed converters at and above resonance. Section IV details a means of comparing capacitively isolated hybrid switched-capacitor converters. Hardware results for individual and SIPO converters are shown in Section V. Section VI concludes this work and summarizes the impact.

II. Topology Derivation

As isolation requires eliminating direct current between the input and output domains of a power converter, the process of capacitively isolating existing non-isolated hybrid switched-capacitor converters must introduce capacitors along any direct current paths between the input and output. Furthermore, the authors define capacitive isolation as occurring only in the absence of switch isolation. As such, the topology formed by the introduction of capacitors along direct current paths must not require any switches to block the isolation voltage. Therefore, the switch voltages should be independent of the isolation voltage. In summary, a topology may only be considered capacitively isolated if capacitors are the element preventing direct current from flowing between input and output terminals, and the only circuit element that experiences isolation voltage. Given this definition of capacitive isolation, a general approach to introducing capacitive isolation into existing hybrid switched-capacitor converters is developed.

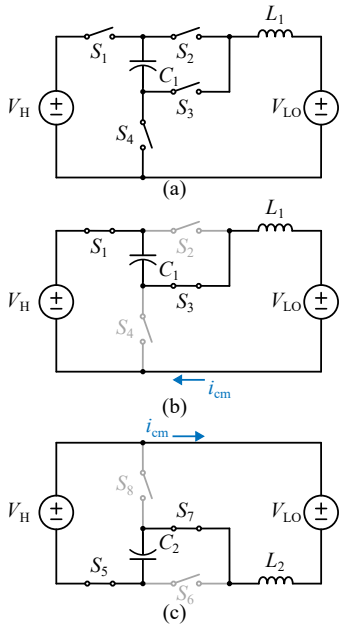


Fig. 2. The 2:1 inductor-at-the-output hybrid switched-capacitor converter shown with the sources connected such that they are (a) common-negative. The connected-phase of the converter is shown for the (b) common-negative and the (c) common-positive configurations of the topology.

A systematic process for introducing capacitive-based isolation into existing hybrid switched-capacitor converters is explained using the 2:1 hybrid switched-capacitor converter with the inductor-at-the-output shown in Fig. 2a. All N-level inductor-at-the-output two-phase hybrid switched-capacitor converters condense to this same converter at $N = 2$ where N is the conversion ratio. This 2:1 converter has a connected stage, shown in Fig. 2b, in which the high-side (V_{H}) sources power and low-side (V_{LO}) sinks power. Despite C_1 blocking direct current between the positive terminals of the sources, this topology is not capacitively isolated due to the direct current path between the negative terminals of the sources, which carries i_{cm} as seen in Fig 2b. Thus, the 2:1 hybrid switched-capacitor converter, and by extension, all N-level converters that condense to this converter are not isolated.

Previous work offers a method of introducing isolation using a reflection of the original converter [12]. While other methods of isolation have been used previously [18], [20], this method allows the derivation of inductor-at-the-output topologies that can operate above resonance. In the reflected variant of the converter, shown in Fig. 2c, the direct current path between the positive terminals carries a current of i_{cm} in the opposite direction. Joining the common-negative node of Fig. 2b and the common-positive node of Fig. 2c effectively cancels the direct current through this branch. Thus, the direct connection joining the voltage sources may be removed as $i_{\text{cm}} = 0$ A. For a SIPO converter, the isolation source represents the necessary isolation voltage defined as $V_{\text{ISO}_y} = \sum_{p=1}^{y-1} V_{\text{IN},p}$ as indexed in Fig. 1. In this work, an isolated converter will be defined a converter with zero current flowing through the isolation source.

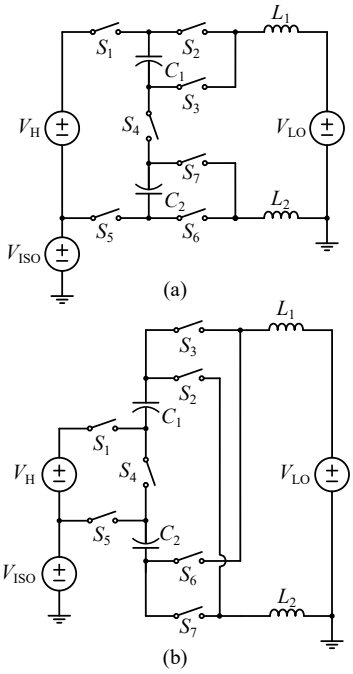


Fig. 3. The simplified topology that results in joining the common-positive and common-negative variants of the 2:1 hybrid switched-capacitor converter. An intermediate step (a) that requires switch isolation. The final variant (b) that provides only capacitive isolation while maintaining charge flow.

Note, voltage sources that, after removing the zero current path, appear in series can be replaced with an equivalent source. Series switches may also be reduced to a single switch. After combining redundant switches and voltages sources, a topology is reached as seen in Fig. 3a. Although the two inductors appear in series, they cannot be combined due to the isolation source, for this would result in the voltage on C_2 being clamped by the isolation voltage. In this topology, switches S_1, S_2, S_5 and S_6 block the isolation voltage. To ensure no switch blocks the isolation voltage and charge flow is maintained, further modifications are applied to reach the topology of Fig. 3b, which provides only capacitive isolation while maintaining charge flow.

The 2:1 capacitively isolated hybrid switched-capacitor converter of Fig. 3b is the basic converter that all N-level capacitively isolated hybrid switched-capacitor converters derived via the approach of this work compress to at $N = 2$. This converter can thus be expanded into the various N-level capacitively isolated inductor-at-the-output hybrid switched-capacitor converters of Fig. 4. A capacitively isolated Cockcroft-Walton converter can also be developed using this method, but was omitted from this work as it requires split-phase control [31] to achieve soft-charging, increasing complexity and making it difficult to compare to other isolated inductor-at-the-output converters. Additionally, this framework can be employed to re-derive the previously presented at resonance capacitively isolated hybrid switched-capacitor converters [14], [15].

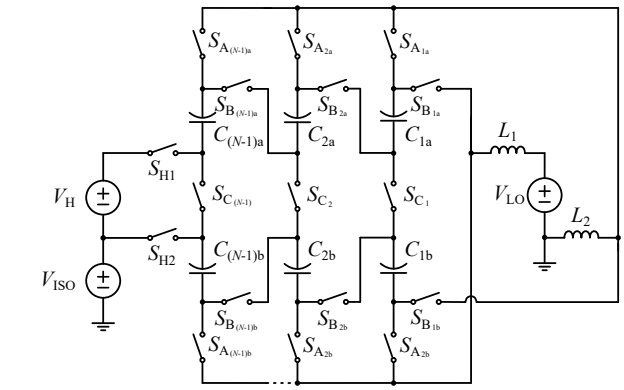
III. Operation Principles

This section describes the general derivation of operation principles for the topologies of Fig. 4. For clarity, the 4:1 capacitively isolated series-parallel converter will be used as reference throughout. Key parameters used in this section and the remainder of this work are summarized in Table I. Additionally, the derived parameters for the series-parallel converter and other converters are listed in Table II.

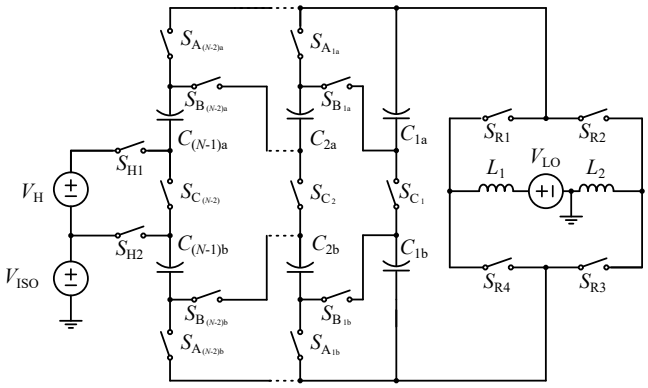
A. Resonant Frequency

The resonant frequency of a hybrid switched-capacitor converter is defined per phase. Thus, the two-phase converters discussed in this work have resonant frequencies $f_{\text{res},1}$ and $f_{\text{res},2}$ for phases one and two respectively. The overall switching period and phase timings are functions of these frequencies as discussed in Section III-D. For each converter, the capacitances are normalized to a capacitance C_0 such that $C_{nk} = c_{nk}C_0$, where c_{nk} is the capacitor scaling factor of capacitor n along the path $k \in \{\text{a}, \text{b}\}$ where $k = \text{a}$ corresponds to the a series capacitors and $k = \text{b}$ corresponds to the b series capacitors. Additionally, the inductances are normalized to an inductance L_0 such that $L_i = l_i L_0$ where l_i is the inductor scaling factor.

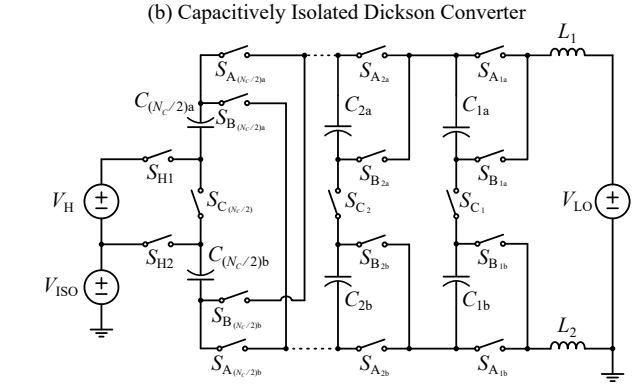
Thus for each phase, a resonant frequency can be determined as in (1) as a function of C_0, L_0, and κ_j, representing the effective LC product. The definition of $\boldsymbol{\kappa}$ presented in (2)



(a) Capacitively Isolated Series-Parallel Converter



(b) Capacitively Isolated Dickson Converter



(c) Capacitively Isolated Fibonacci Converter

Fig. 4. Capacitively isolated variants of the (a) series-parallel converter, (b) Dickson converter and (c) Fibonacci converter shown at a generalized conversion ratio of N:1.

is more general than that of [30] as it incorporates converters with multiple inductors.

$$f_{\text{res},j} = \frac{1}{2\pi\sqrt{\kappa_j C_0 L_0}} \tag{1}$$

$$\kappa_j = \frac{C_{\text{eff},j} L_{\text{eff},j}}{C_0 L_0} \tag{2}$$

The derivation of the converters discussed in Section II, ensures that zero current flows though the isolation source when the components are symmetrically sized e.g $C_{n\text{a}} = C_{n\text{b}} = C_n = c_n C_0$ for all n and $L_1 = L_2 = L_0$. The capacitor scaling vectors, $\boldsymbol{c}$, for each converter are listed in Table II. Thus,

TABLE I
DEFINITION OF KEY TERMS

N	Conversion ratio.
N_p	Total number of phases.
N_c	Total number of flying capacitors.
N_l	Total number of inductors.
N_s	Total number of switches.
n	Numeric index of flying capacitors and switches.
k	Index of flying capacitors where $k \in \{\text{a}, \text{b}\}$.
j	Phase index.
i	Numeric index of inductors.
$H_{k,jn}$	Normalized charge flow for capacitor n in phase j along path k.
$H_{L,ji}$	Normalized charge flow for inductor i in phase j.
$\boldsymbol{v}$	Capacitor mid-range voltage vector normalized to the high-side voltage.
c_{nk}	Capacitor scaling factor of capacitor n along path k where $C_{nk} = c_{nk} C_0$
l_i	Inductor scaling factor of inductor i where $L_i = l_i L_0$.
κ_j	The effective LC product in phase j normalized to $L_0 C_0$.
$\boldsymbol{\tau}$	Phase timing vector normalized to the total switching period.
$q_{n_k,j}$	Charge conducted in phase j by capacitor n along path k.
$q_{L,j}$	Charge entering the low-side source in phase j.
q_{HI}	Charge exiting the high-side source during the connected phase.

the inductors are effectively in series when no current flows through the isolation source. As such the resonant frequency can be determined by eliminating the isolation voltage and finding the Thevenin equivalent impedance from the low-side port. Table II presents the vector $\boldsymbol{\kappa}$ for the converters of Fig. 4.

The effective resonant frequency is consistent with the non-isolated inductor-at-the-output variant of a topology given consistent component sizing [30].

1) Example: 4:1 Series-Parallel Converter: For the 4:1 series-parallel converter, the per phase resonant frequencies can be determined using Fig. 6. In the series-parallel converter, the capacitors are sized such that $C_0 = C_{1\text{a}} = C_{1\text{b}} = \cdots = C_{N_c/2\text{a}} = C_{N_c/2\text{b}}$ and the inductors are equal.

In phase one, the capacitors are series connected forming effective an capacitance of $\frac{C_0}{6}$ as seen in Fig. 6a when the current though the isolation source is considered negligible. As the effective inductance is $2L_0$, the resonant frequency for this phase is $f_{\text{res},1} = \frac{1}{2\pi\sqrt{\frac{1}{3}L_0 C_0}}$. Thus, κ_1 is equal to one-third.

In phase two, the inductors are in series again forming an effective inductance of $2L_0$ and the effective capacitance is $\frac{3}{2}C_0$. The phase two resonant frequency is $f_{\text{res},2} = \frac{1}{2\pi\sqrt{3L_0 C_0}}$, yielding a κ_2 of three. Therefore, $\boldsymbol{\kappa}$ can be represented as a vector $\boldsymbol{\kappa} = \begin{bmatrix} \frac{1}{3} & 3 \end{bmatrix}$.

B. Capacitor Mid-range Voltages

Initial Kirchoff's Voltage Law (KVL) analysis of capacitor voltages results in under-constrained mid-range voltages for the capacitively isolated topologies. Each capacitor's voltage

can be expressed as in (3), where α_{n_k} and β_{n_k} are unknown scaling factors.

$$V_{\mathrm{C}_{nk}} = \alpha_{n_k} V_{\mathrm{H}} + \beta_{n_k} V_{\mathrm{ISO}} \tag{3}$$

However, the output capacitance of switches of S_{H1} and S_{H2} constrains the voltages of $C_{(N_c/2)a}$ and $C_{(N_c/2)b}$ described in (4), where N_c is the total number of capacitors for a given conversion ratio, for all of the converter shown in Fig. 4.

$$V_{\mathrm{C}_{n_k}} = \begin{cases} \alpha_{n_k} V_{\mathrm{H}} & \text{for } n < \frac{N_c}{2},\ k \in \{\mathrm{a,b}\} \\ \alpha_{n_\mathrm{b}} V_{\mathrm{H}} - \beta_{n_\mathrm{b}} V_{\mathrm{ISO}} & \text{for } n = \frac{N_c}{2} \\ \alpha_{n_\mathrm{a}} V_{\mathrm{H}} + \beta_{n_\mathrm{a}} V_{\mathrm{ISO}} & \text{for } n = \frac{N_c}{2} \end{cases} \tag{4}$$

To simplify the analysis it is assumed that the C_{oss} of the switches, shown as $C_{\mathrm{oss,H1}}$ and $C_{\mathrm{oss,H2}}$ in Fig. 5, are matched. Therefore, the scaling factors of (4) for the terminal capacitors are $\alpha_{(N_c/2)_\mathrm{a}} = \alpha_{(N_c/2)_\mathrm{b}}$ and $\beta_{(N_c/2)_\mathrm{a}} = \beta_{(N_c/2)_\mathrm{b}} = 1$. For the remaining capacitors, the minimum energy state of capacitors in series indicates that $\alpha_{n_\mathrm{a}} = \alpha_{n_\mathrm{b}}$. However, deviations from this state may occur due to practical implementation factors such component mismatch and layout asymmetries. A thorough investigation into the effect of C_{oss} on the capacitor mid-range voltages is out of scope of this work.

The mid-range voltages can be expressed in a mid-range voltage vector, $\boldsymbol{v}$, which is normalized to V_{H}. The mid-range voltage vector for each converter is expressed in Table II. Note the analysis in Table II assumes that $C_{\mathrm{oss,\ H1}} = C_{\mathrm{oss,\ H2}}$ and voltage is split evenly between series capacitors of equal capacitance.

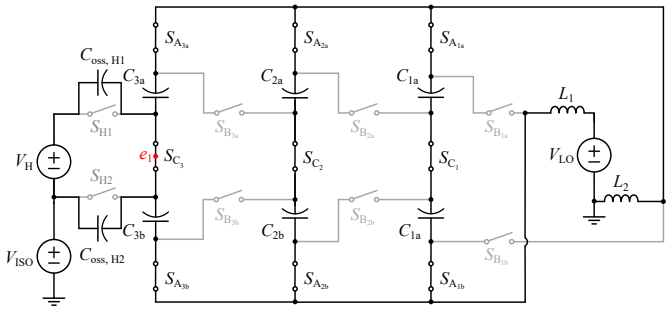


Fig. 5. The 4:1 capacitively isolated series-parallel converter in phase two with C_{oss} for high side switches S_{H1} and S_{H2} depicted. The node voltage e_1 shown in red is $e_1 = \frac{V_{\mathrm{H}}}{2} + V_{\mathrm{ISO}}$ when the switch capacitances are equal.

1) Example: 4:1 Series-Parallel Converter: Figure 5 shows the 4:1 series-parallel converter with C_{oss} shown for the relevant 'off' (b series) switches in phase two. The C_{oss}, which are several orders of magnitude smaller that the flying capacitors C_{1k} - C_{3k} for $k \in \{\mathrm{a,b}\}$, corresponding to the switches $S_{B_{nb}}$ for all n, are in parallel with a flying capacitor and can thus be omitted from Fig. 5. The loop formed by V_{H} and the C_{oss} of S_{H1} and S_{H2} determines the node voltage $e_1 = \frac{V_{\mathrm{H}}}{2} + V_{\mathrm{ISO}}$ and fully defines the capacitor mid-range voltages $C_{3\mathrm{a}}$ and $C_{3\mathrm{b}}$. To determine remaining the capacitor mid-range voltages, it is assumed that the capacitor voltages are in steady state and maintain a minimum energy state. In the case of the series-parallel converter, this indicates that $\alpha_{n_k} = \frac{1}{2}$ for all $n_k < \frac{N_c}{2}$. In practice, imbalances in components such as C_{oss}, $R_{\mathrm{ds,on}}$, flying capacitance, and commutation loop inductance will affect the exact values of α_{n_k}. Section V will confirm this analysis with experimentally derived capacitor voltages.

C. Charge Flow

Charge flow enables understanding of converter conversion ratio, capacitor voltage ripple and inductor current ripple using a charge flow matrix, $H_{k,jn}$. Under a steady-state assumption, the capacitors must be charge balanced (e.g the charge flowing into the capacitor must equal that flowing out of the capacitor). For two-phase converters this can be expressed simply as $q_{n_k,1} = -q_{n_k,2}$. The topology derivation process discussed in Section II ensures charge balance. Due to the symmetry of the converters, the characteristic vectors of the a series and b series capacitors are equal ($H_{\mathrm{a},jn} = H_{\mathrm{b},jn}$). The characteristic charge flow matrix $H_{k,jn}$, seen in (5), will be simplified such that $H_{jn} = H_{\mathrm{a},jn} = H_{\mathrm{b},jn}$. Note that the polarity of charge flow is dependent on choice of capacitor polarity, so this simplification will not hold for all choices of capacitor polarity.

$$H_{jn} = \begin{bmatrix} \frac{q_{1,1}}{q_{\mathrm{HI}}} & \frac{q_{2,1}}{q_{\mathrm{HI}}} & \cdots & \frac{q_{N_C/2,1}}{q_{\mathrm{HI}}} \\ -\frac{q_{1,1}}{q_{\mathrm{HI}}} & -\frac{q_{2,1}}{q_{\mathrm{HI}}} & \cdots & -\frac{q_{N_C/2,1}}{q_{\mathrm{HI}}} \end{bmatrix} \tag{5}$$

The conversion ratio, N, of a given converter can be calculated using (6) where j is the phase index, $q_{\mathrm{HI},j}$ is the charge per phase leaving the high-side source, and $q_{L,j}$ is the per phase charge entering the low-side source. For all converters discussed in this work, there is only one phase in which the high-side source is connected. Thus, total charge leaving the high-side source can be expressed as q_{HI}.

$$N = \frac{\sum_j q_{L,j}}{q_{\mathrm{HI}}} \tag{6}$$

As the isolation source has zero current flow, the charge entering the low-side source, $q_{L,j}$, is also the magnitude of charge flow for L_1 and L_2.

Charge flow may also be used to characterize the capacitor voltage ripple. Using the charge flow vectors of Table II, the relative voltage ripple of the capacitors can be determined. The capacitor ripple for phase j can be expressed an in (7) for a given capacitor C_{nk}. Note that due to the symmetry of the topology construction, $C_{n\mathrm{a}} = C_{n\mathrm{b}} = C_n$ and $q_{n_\mathrm{a},j} = q_{n_\mathrm{b},j} = q_{n,j}$ for all n.

$$\Delta v_{n,j} = \frac{q_{n,j}}{C_n} = \frac{H_{jn} q_{\mathrm{HI}}}{c_n C_0} \tag{7}$$

1) Example: 4:1 Series-Parallel Converter: The charge flow of a 4:1 capacitively isolated series-parallel converter is shown in Fig. 6 for both operation phases. For the chosen capacitors polarity $H_{\mathrm{a},jn} = H_{\mathrm{b},jn} = H_{jn}$. The resultant charge flow vector is shown in (8).

$$H_{\mathrm{a},jn} = H_{\mathrm{b},jn} = H_{jn} = \begin{bmatrix} 1 & 1 & \cdots & 1 \\ -1 & -1 & \cdots & -1 \end{bmatrix} \tag{8}$$

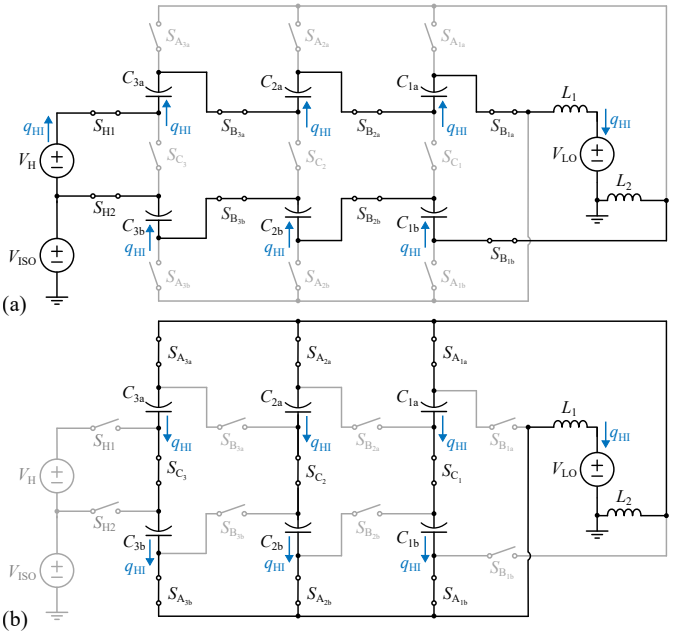


Fig. 6. Two-phase operation of the 4:1 capacitively isolated series-parallel converter for phases (a) one and (b) two. The per-phase charge flow is shown in black.

For the series-parallel converter of Fig. 6 operated with two phases, the conversion ratio derivation is detailed in (9).

$$N = \frac{q_{L,1} + q_{L,2}}{q_{\text{HI}}} = \frac{q_{\text{HI}} + 3q_{\text{HI}}}{q_{\text{HI}}} = 4 \tag{9}$$

Furthermore, each capacitor experiences the same voltage ripple since the charge flow and capacitances are equal for all n.

D. Phase Timings

1) At Resonance: To determine the duration of time spent in each phase, the at resonance converter operation can be analyzed. At resonance, the inductor current is half-wave resonant as shown in Fig 7. As such, the phase duration t_j can be expressed as in (10) where T is the total period duration and τ_j represents the fraction of the total period spent in phase j.

$$\tau_j = \frac{t_j}{T} \tag{10}$$

For at-resonant operation, the time spent in phase j can be represented as seen in (11).

$$t_j = \frac{T_j}{2} = \frac{\pi}{\omega_j} \tag{11}$$

The at resonance period T_{res} can then be expressed an in (12).

$$T_{\text{res}} = \sum_j t_j \tag{12}$$

2) Above Resonance: Above resonance, the inductor current transition happens before the zero crossing is reached as seen in Fig. 8. For simplicity it is assumed that, the phase transitions always occur at the same inductor current value. This above-resonant operation has resonant-like behavior with an operation frequency higher than resonance. A scalar term, Γ, expressed mathematically in (13), quantifies how far above the resonance frequency, f_{res}, the converter is being switched, f_{sw}.

$$\Gamma = \frac{f_{\text{sw}}}{f_{\text{res}}} = \frac{T_{\text{res}}}{T} \tag{13}$$

Equation (11) can be updated to hold for all values of Γ where the phase durations can be expressed in terms of Γ as in (14). Note that for $\Gamma = 1$, e.g at-resonant operation, (11) and (14) are equivalent.

$$t_j = \frac{T_j}{2\Gamma} = \frac{\pi}{\omega_j \Gamma} \tag{14}$$

When normalized to T_j, the phase normalization parameter $\boldsymbol{\tau}$ is expressed in terms of relevant parameters in Table II.

3) Example: 4:1 Series-Parallel Converter: Using (14) and the 4:1 capacitively isolated resonant frequency analysis, the phase timings can be determined for phases one and two as $t_j = \frac{\pi\sqrt{\kappa_j L_0 C_0}}{\Gamma}$. This results in at-resonant ($\Gamma = 1$) duration of $t_1 = \frac{\pi\sqrt{L_0 C_0}}{\sqrt{3}}$ and $t_2 = \pi\sqrt{3L_0 C_0}$. The total period, T is the sum of t_1 and t_2 and can be expressed as $T = \frac{4\pi}{\sqrt{3}}\sqrt{L_0 C_0}$. The phase normalization parameter for each phase is $\tau_1 = \frac{1}{4}$ and $\tau_2 = \frac{3}{4}$. The phase normalization can be expressed as $\boldsymbol{\tau} = \begin{bmatrix} \frac{1}{4} & \frac{3}{4} \end{bmatrix}$. While the values of t_j and T depend on the

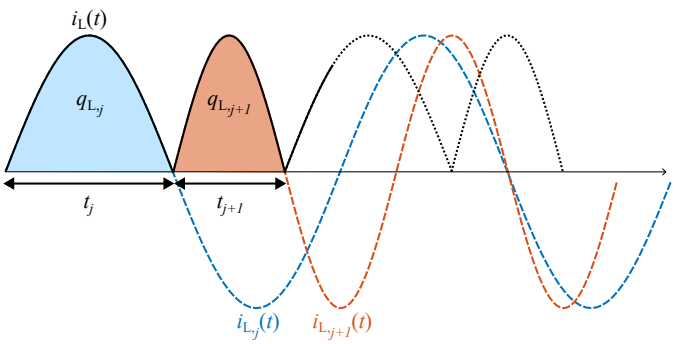


Fig. 7. The at resonance inductor current $i_L(t)$ with relevant parameters indicated. The per-phase inductor currents $i_{L,j}(t)$ and $i_{L,j+1}(t)$ are shown in black and red respectively.

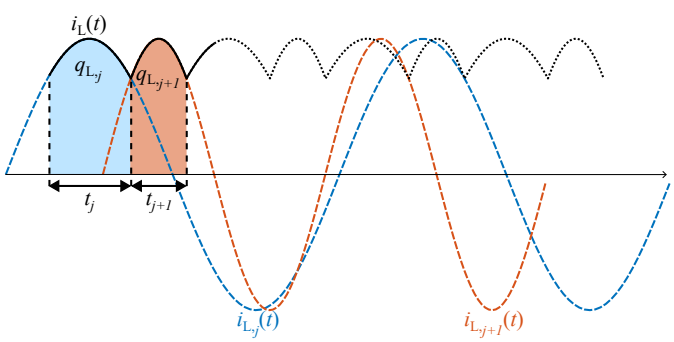


Fig. 8. The above resonance inductor waveform $i_L(t)$ as a piecewise combination of the per-phase resonant inductor current waveforms $i_{L,j}(t)$ (black) and $i_{L,j+1}(t)$ (red).

choice of Γ, the phase normalization parameter is independent of Γ and depends only on level count.

E. Inductor Current

As no current flows through the isolation voltage, the currents through each inductor are equal in both phases; thus, the inductor current can be analyzed for both inductors simultaneously. The inductor current can be expressed as $i_L(t) = \frac{dq}{dt}$. Consequently, the inductor charge flow $q_{L,j}$ can be found as a function of the inductor current as in (15).

$$q_{L,j} = \int_{t_j}^{t_{j+1}} i_{L,j}(t)\ dt \tag{15}$$

The per phase inductor charge can be determined through charge flow [32]. The normalized inductor charge flow matrix, $H_{L,ji}$, relates the per phase inductor charge to q_{HI} as seen in (16). Note that $q_{L,j1} = q_{L,j2} = q_{L,j}$, thus the columns of the inductor charge flow matrix are equal.

$$H_{L,ji} = \frac{q_{L,ji}}{q_{\text{HI}}} \tag{16}$$

Resonant-like converter operation indicates that the inductor current is sinusoidal in nature. The steady-state undamped per phase inductor current for resonant operation is expressed in (17). At-resonant operation results in phase transitions occurring at the zero crossings of the inductor current [33]. Figure 7 shows the phase one and phase two inductor current waveforms under steady-state undamped resonant operation in black ($i_{L,j}$) and red ($i_{L,j+1}$) with adequate phase shifts for the converter waveform shown in black (i_L) to achieve ZCS.

$$i_{L,j}(t) = I_{\text{pk},j} \sin\left(\omega_j t + \theta_j\right) \tag{17}$$

Expressions for inductor currents $i_{L,1}$ and $i_{L,2}$ in terms of I_{out} and as a function of Γ for two phase operation are shown in (18) and (19), respectively. The derivation of $i_{L,j}$, at and above resonance is presented in the Appendix.

$$i_{L,1}(t) = \frac{I_{\text{out}}\pi}{2\Gamma \sin\left(\frac{\pi}{2\Gamma}\right)} \sin\left(\omega_1 t\ +\ \frac{\pi\ (\Gamma-1)}{2\Gamma}\right) \tag{18}$$

$$i_{L,2}(t) = \frac{I_{\text{out}}\pi}{2\Gamma \sin\left(\frac{\pi}{2\Gamma}\right)} \sin\left(\omega_2 t\ +\ \frac{\pi\ (\Gamma-1)}{2\Gamma} - \frac{\omega_2\pi}{\omega_1\Gamma}\right) \tag{19}$$

The normalized inductor peak, I_{pk}, peak to peak, $I_{\text{pk,pk}}$, and RMS, I_{RMS}, currents are plotted as a function of Γ in Fig. 9. At $\Gamma < 2$, the inductor $I_{\text{pk,pk}}$, I_{pk}, and I_{RMS} decrease rapidly while at values $\Gamma > 2$ the rate of decline decreases and eventually plateaus. While increasing Γ provides component stress and sizing benefits, due to the reduction in these currents, there are marginal benefits to increasing Γ to values larger than two. Furthermore, increasing Γ proves disadvantageous as it leads to increased switching losses. Thus, Fig. 9 motivates limiting above resonance operation to less than twice the resonant frequency.

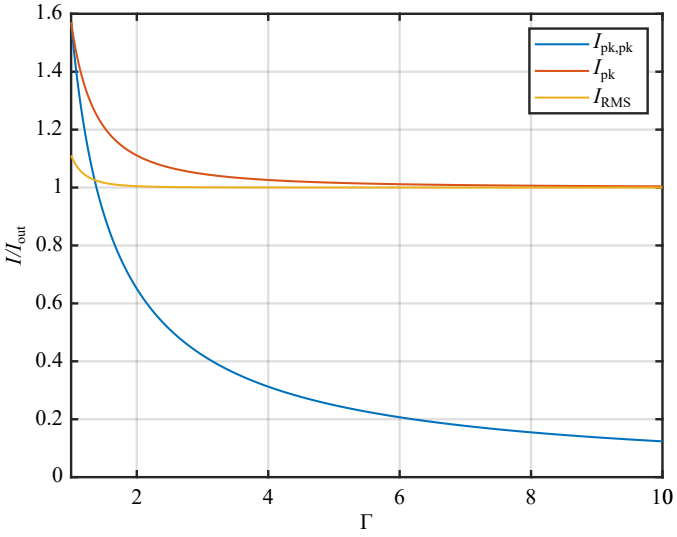


Fig. 9. Relevant component sizing parameters, $I_{\text{pk,pk}}$, I_{pk}, and I_{RMS} normalized to I_{out} as a function of Γ.

F. Switch Voltages

The switch voltages can be expressed as a sum of a dc term and a ripple term as seen in (20). The voltage on a given switch depends on the difference in the switches' drain and source voltages during the phase when it is blocking voltage.

$$v_{\text{ds}} = V_{\text{dc}} + \Delta v \tag{20}$$

The switch voltage including ripple can be derived for each converter as seen in Table III.

Furthermore, the switch voltages place a limit on the power processed via capacitor-ripple-induced clamping [30], [34]. The capacitor ripple can induce reverse voltages on the switches and consequently force undesirable reverse conduction. The maximum power processed due to this constraint is presented for each converter in Table IV.

1) Example: 4:1 Series-Parallel Converter: For the 4:1 capacitively isolated series-parallel converter of Fig. 6, the switches are grayed out during the phase in which they are off. To calculate the v_{ds} of a given switch, KVL can be performed around a loop containing the switch of interest. For $S_{A_{1a}}$, this could be the loop including $S_{A_{1a}}$, L_1, V_{LO}, and L_2. Both the high- and low-side voltages are assumed to be purely dc. As the average inductor voltage is zero, the voltage of the switch $V_{A_{1a}}$ depends only on the output voltage and the inductor voltage ripple, Δv_L, as shown in (21).

$$\begin{aligned} v_{A_{1a}} = V_{\text{LO}} + 2\Delta v_L &= V_{\text{LO}} + \max_{j\in[N_p]}\left\{\frac{H_{L,ji} q_{\text{HI}}}{\kappa_j \Gamma C_0}\right\} \\ &= V_{\text{LO}} + \frac{(N-1) q_{\text{HI}}}{\Gamma C_0} \end{aligned} \tag{21}$$

G. Switch Currents

The switch currents can be expressed in terms of the inductor currents derived in Sections III-E.

TABLE II
CHARACTERISTIC VECTORS FOR CAPACITIVELY ISOLATED HYBRID SWITCHED-CAPACITOR CONVERTERS

Topology	**Series-parallel** $N \in \{\mathbb{N} \geq 2\}$	**Dickson (odd N)** $N \in \{\mathbb{N} \geq 2\}$	**Fibonacci** $N \in \{F_m : m \in \mathbb{N} \geq 3\}$, $F_x = (1, 1, 2, 3, 5, 8, 13...)$
N_p	2	2	2
N_c	$2(N-1)$	$2(N-1)$	$2(m-2)$
N_l	2	2	2
N_s	$5N-3$	$5N-3$	$5m-8$
$H_{[N_p \times N_c]}$	$\begin{bmatrix} 1 & 1 & \cdots & 1 \\ -1 & -1 & \cdots & -1 \end{bmatrix}$	$\begin{bmatrix} -1 & -1 & 1 & \cdots -1 & 1 & 1 \\ 1 & 1 & -1 & \cdots 1 & -1 & -1 \end{bmatrix}$	$\begin{bmatrix} -F_{m-2} & F_{m-3} & \cdots & \pm F_2 & \pm F_1 & \pm F_1 \\ F_{m-2} & -F_{m-3} & \cdots & \pm F_2 & \pm F_1 & \pm F_1 \end{bmatrix}$
$H_{[N_p \times N_l]}$	$\begin{bmatrix} 1 & 1 \\ N-1 & N-1 \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2} & \frac{N+1}{2} \\ \frac{N-1}{2} & \frac{N-1}{2} \end{bmatrix}$	$\begin{bmatrix} F_{(m-1)} & F_{(m-1)} \\ F_{(m-2)} & F_{(m-2)} \end{bmatrix}$
$\boldsymbol{v}_{[1 \times N_c/2]\text{a}}$	$\begin{bmatrix} \frac{1}{2N} & \cdots & \frac{1}{2N} & \frac{1}{2} + \frac{V_{iso}}{V_H} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{2N} & \frac{2}{2N} & \cdots & \frac{N-2}{2N} & \frac{N-1}{N} + \frac{V_{iso}}{V_H} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2N} & -\frac{2}{2N} & -\frac{3}{2N} & \cdots & -\frac{F_{m-1}}{2N} & \frac{V_{iso}}{V_H} + 1 - \frac{1-\sum_{i,}^{m-3} \frac{F_{i+1}}{2}}{N} \end{bmatrix}$
$\boldsymbol{v}_{[1 \times N_c/2]\text{b}}$	$\begin{bmatrix} \frac{1}{2N} & \cdots & \frac{1}{2N} & (\frac{1}{N} - \frac{1}{2}) - \frac{V_{iso}}{V_H} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{2N} & \frac{2}{2N} & \cdots & \frac{N-2}{2N} & -\frac{V_{iso}}{V_H} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2N} & -\frac{2}{2N} & -\frac{3}{2N} & \cdots & -\frac{F_{m-1}}{2N} & -\frac{V_{iso}}{V_H} + \frac{\sum_{i,}^{m-3} \frac{F_{i+1}}{2}}{N} \end{bmatrix}$
$\boldsymbol{c}_{[1 \times N_c]}$	$\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{N-1}{N-1} & \frac{N-1}{2} & \frac{N-1}{N-3} & \cdots & \frac{N-1}{2} & \frac{N-1}{N-1} \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}$
$\kappa_{[N_p \times 1]}$	$\begin{bmatrix} \frac{1}{N-1} \\ N-1 \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2} & \frac{N+1}{2} \\ \frac{(N-1)^2}{2(N+1)} & \frac{(N-1)^2}{2(N+1)} \end{bmatrix}$	$\begin{bmatrix} \frac{F_{m-1}}{F_{m-2}} & \frac{F_{m-1}}{F_{m-2}} \\ \frac{F_{m-2}}{F_{m-1}} & \frac{F_{m-2}}{F_{m-1}} \end{bmatrix}$
$\tau_{[N_p \times 1]}$	$\begin{bmatrix} \frac{1}{N} \\ \frac{N-1}{N} \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2N} \\ \frac{N-1}{2N} \end{bmatrix}$	$\begin{bmatrix} \frac{F_{m-1}}{F_m} \\ \frac{F_{m-2}}{F_m} \end{bmatrix}$

1) Example: 4:1 Series-Parallel Converter: Using charge flow as in [32], it is determined that each capacitor discharges or charges by an equal amount, q. Thus, the capacitor currents and consequently 'on' switch currents are of equal magnitude. In phase two, there are $N-1$ parallel combinations of capacitors. As such, the phase two 'on' switch currents are $\frac{i_{L,2}}{N-1}$. The generalized drain-to-source switch currents are shown in (22).

$$I_{ds,x} = \begin{cases} i_{L,1} & \text{for } x = [B_{n_a}, B_{n_b}, H1, H2] \\ \frac{i_{L,2}}{N-1} & \text{for } x = [A_{n_a}, A_{n_b}, C_n] \end{cases} \tag{22}$$

IV. COMPARISON

This section aims to provide designers insight regarding the tradeoffs associated with the topologies presented in this work as well as existing capacitively isolated hybrid switched-capacitor converters. The capacitively isolated Dickson converter [14] has previously been demonstrated in SIPO converter architecture [8]. This resonant tank converter has a conversion ratio of N for $N \geq 2$ at even values of N. Thus it will be referred to in this work as the even Dickson converter. The even Dickson converter differs from the capacitively isolated converters present in this work as all the capacitor mid-range voltages depend on the isolation voltage ($\beta_n = 1$ for $n \leq N$ as defined in (3)). Furthermore, while this converter cannot operate above resonance, the capacitor voltage ripple cancels such that the switch voltage is independent of load. Thus, it provides an interesting comparison to the converters of this work.

A. Passive Component Sizing

A comparison of capacitively isolated converter topologies via passive component sizing was conducted according to the analytical method presented in [30], in which the total passive volume of a converter is determined by relating the peak energy stored in each passive component to the volume using a capacitor volumetric energy density factor (ρ_c), an inductor volumetric energy density factor (ρ_l), and a volumetric energy density ratio ($\rho = \frac{\rho_c}{\rho_l}$). While the volumetric energy density was chosen in this work, other conversion factors may be used depending on the metric the designer wishes to compare. Previous work developed generalized equations for capacitor volume in terms of the vectors of Table II. The maximum peak energy stored in the capacitors, as derived by [30] is shown in (23). Note that for capacitively isolated topologies, the mid-range voltage vector, $\boldsymbol{v}$, is a function of the isolation voltage.

$$\begin{aligned} E_{C,\text{pk},nk} &= \max_{j \in [N_p]} \{\frac{1}{2} C_n V_{\text{pk},C_n}^2\} \\ &= \frac{1}{2} \boldsymbol{c}_n C_0 (\boldsymbol{v}_{nk} V_\text{H} + \frac{1}{2} \Delta v_{n_k})^2 \end{aligned} \tag{23}$$

TABLE III
SWITCH VOLTAGES FOR N-LEVEL CAPACITIVELY ISOLATED CONVERTERS AS SEEN IN FIG. 4.

Series-Parallel			
	dc	Voltage Ripple	
Normalization Factor	V_{H}	$\frac{q_{\text{HI}}}{C_0}$	
$S_{\text{A}_{ia}}$, $S_{\text{A}_{ib}}$	$\frac{1+i}{2N}$	$(N-1)-\frac{(i-1)}{2}$	$1 \le i \le N$
$S_{\text{B}_{1a}}$, $S_{\text{B}_{1b}}$	$\frac{1}{N}$	1	$i = 1$
$S_{\text{B}_{ia}}$, $S_{\text{B}_{ib}}$	$\frac{1}{2N}$	$\frac{1}{2}$	$2 \le i \le N$
S_{C_i}	$\frac{i+1}{N}$	$N-i$	$1 \le i \le N-2$
$S_{\text{C}_{N-1}}$	1	-	$i = N-1$
$S_{\text{H}i}$	$\frac{1}{2}$	-	$1 \le i \le 2$
Fibonacci			
	dc	Voltage Ripple	
Normalization Factor	V_{H}	$\frac{q_{\text{HI}}}{C_0}$	
$S_{\text{A}_{ia}}$, $S_{\text{B}_{ia}}$, $S_{\text{A}_{ib}}$, $S_{\text{B}_{ib}}$	$\frac{F_{i+1}}{2N}$	$\frac{F_{(m-i-1)}}{2}$	$1 \le i < \frac{N_{\text{c}}}{2}$
$S_{\text{A}_{N_{\text{c}}/2a}}$, $S_{\text{A}_{N_{\text{c}}/2b}}$	$\frac{F_{m-1}}{N}$	1	$i = \frac{N_{\text{c}}}{2}$
$S_{\text{B}_{N_{\text{c}}/2a}}$, $S_{\text{B}_{N_{\text{c}}/2b}}$	$\frac{F_{m-2}}{N}$	1	$i = \frac{N_{\text{c}}}{2}$
S_{C_i}	$\frac{F_i}{N}$	F_{m-i}	$1 \le i < \frac{N_{\text{c}}}{2}$
$S_{C_{N_c/2}}$	1	-	$i = \frac{N_{\text{c}}}{2}$
$S_{\text{H}i}$	$\frac{1}{2}$	-	$1 \le i \le 2$
Dickson			
	dc	Voltage Ripple	
Normalization Factor	V_{H}	$\frac{q_{\text{HI}}}{C_0}$	
$S_{\text{A}_{ia}}$, $S_{\text{A}_{ib}}$	$\frac{i}{2N}$	$\begin{cases} \frac{i}{2(N-1)} & \text{for } i \text{ even} \\ \frac{N-i}{2(N-1)} & \text{for } i \text{ odd} \end{cases}$	$1 \le i \le N-2$
$S_{\text{B}_{ia}}$, $S_{\text{B}_{ib}}$	$\frac{1}{2N}$	$\begin{cases} \frac{N+1}{2(N-1)} & \text{for } i \text{ even} \\ \frac{1}{2} & \text{for } i \text{ odd} \end{cases}$	$1 \le i \le N-2$
S_{C_i}	$\frac{i+1}{N}$	$\begin{cases} \frac{i+1}{2(N-1)} & \text{for } i \text{ odd} \\ \frac{N-i-1}{2(N-1)} & \text{for } i \text{ even} \end{cases}$	$1 \le i \le N-2$
$S_{\text{C}_{N-1}}$	1	-	$i = N-1$
$S_{\text{H}i}$	$\frac{1}{2}$	-	$1 \le i \le 2$
$S_{\text{R}i}$	$\frac{1}{N}$	$\begin{cases} 1 & \text{for } i \text{ odd} \\ \frac{N+1}{N-1} & \text{for } i \text{ even} \end{cases}$	$1 \le i \le 4$

The total peak capacitor energy stored is expressed in (24).

$$E_{C,\text{tot}} = \sum_{k\in\{\text{a,b}\}} \sum_{n=1}^{N_c/2} E_{C,\text{pk}_{nk}} \tag{24}$$

Substituting (23) into (24) yields (25)

$$E_{C,\text{tot}} = \frac{C_0 V_{\text{H}}^2}{2} A_1 + \frac{q_{\text{HI}} V_{\text{H}}}{2} A_2 + \frac{q_{\text{HI}}^2}{8C_0} A_3 \tag{25}$$

The relevant parameters A_1, A_2, and A_3 are shown in (26), (27), and (28) respectively. Note that while the equation for total peak capacitor energy stored, (25), is expressed similarly in [30], the parameters A_1, A_2, and A_3 are redefined in this work.

$$A_1 = \sum_{k\in\{\text{a,b}\}} \sum_{n=1}^{N_c/2} c_n v_{nk}^2 \tag{26}$$

TABLE IV
MAXIMUM POWER PROCESSING CAPABILITIES OF CAPACITIVELY ISOLATED INDUCTOR-AT-THE-OUTPUT CONVERTERS.

Series-Parallel	$\frac{V_{\text{H}}^2 C_0 f_{\text{sw}}}{N(N-1)}$
Fibonacci	$\frac{V_{\text{H}}^2 C_0 f_{\text{sw}}}{N F_{m-1}}$
Dickson	$\frac{(N-1) V_{\text{H}}^2 C_o f_{\text{sw}}}{N(N+1)}$

$$A_2 = \sum_{k\in\{\text{a,b}\}} \sum_{n=1}^{N_c/2} H_{n1} v_{nk} \tag{27}$$

$$A_3 = \sum_{k\in\{\text{a,b}\}} \sum_{n=1}^{N_c/2} \frac{H_{n1}^2}{c_n} \tag{28}$$

The maximum peak energy stored in each capacitors can be related to the total passive volume of the capacitors using the capacitor volumetric density factor as seen in (29).

$$\text{Vol}_{C,\text{tot}} = \frac{E_{C,\text{tot}}}{\rho_c} \tag{29}$$

For the inductor volume, the peak energy stored in the inductors is calculated using the inductor current derivation of Section III-E and is shown in (30). The maximum peak energy stored in the inductors is then converted to volume using the inductor volumetric energy density.

$$\begin{aligned} E_{L,\text{pk},i} &= \max_{j\in[N_p]} \left\{ \frac{1}{2} L_0 I_{\text{pk},j}^2 \right\} \\ &= \max_{j\in[N_p]} \left\{ \frac{H_{L,ji}^2 \Gamma^2 q_{\text{HI}}^2}{8 C_0 \kappa_j \sin^2\left(\frac{\pi}{2\Gamma}\right)} \right\} \end{aligned} \tag{30}$$

The total peak inductor energy over all inductors is then

$$\begin{aligned} E_{L,\text{tot}} &= \sum_{i=1}^{N_l} E_{L,\text{pk},i} \\ &= \frac{q_{\text{HI}}^2}{2C_0} B_1 \end{aligned} \tag{31}$$

where B_1 is as defined in (32).

$$B_1 = \sum_{i=1}^{N_l} \max_{j\in[N_p]} \frac{H_{L,ji}^2}{4\kappa_j \sin^2\left(\frac{\pi}{2\Gamma}\right)} \tag{32}$$

The total inductor passive volume is expressed in (33)

$$\text{Vol}_{L,\text{tot}} = \frac{E_{L,\text{tot}}}{\rho_l} \tag{33}$$

Thus, the total passive volume is the sum of the total capacitor and inductor passive volumes, which is expressed in (34).

$$\text{Vol}_{\text{tot}} = \text{Vol}_{C,\text{tot}} + \text{Vol}_{L,\text{tot}} \tag{34}$$

Given this formulation of the parameters A_1, A_2, A_3, and B_1, the equations for minimum normalized capacitance (C_0^*), minimum total passive volume ($\text{Vol}_{\text{tot}}^*$), and normalized minimum passive volume (M_{Vol}^*) from [30] may be used to solve for these metrics for the capacitively isolated topologies of this

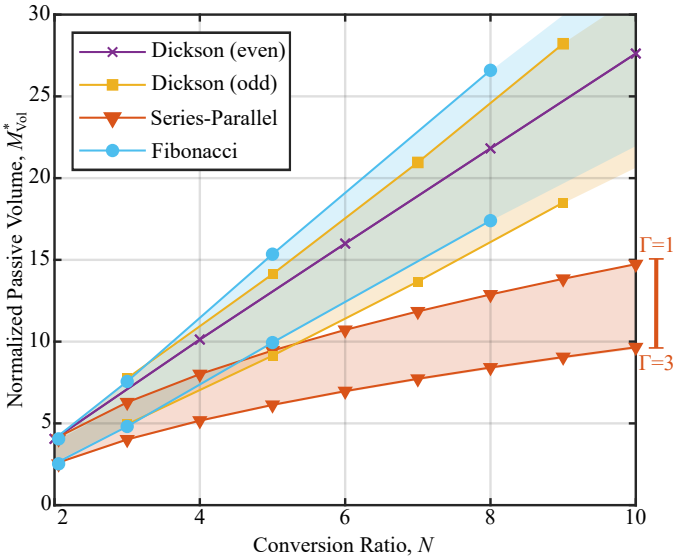


Fig. 10. Normalized passive volume, M^*_{Vol}, versus conversion ratio, N, of capacitively isolated hybrid switched-capacitor converters operating at and above resonance for $V_{\text{ISO}} = 0$.

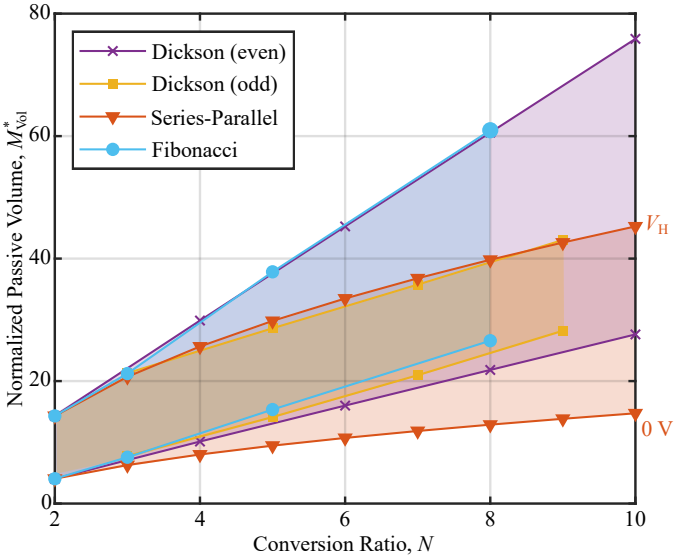


Fig. 11. The normalized passive volume, M^*_{Vol}, versus conversion ratio, N, of capacitively isolated hybrid switched-capacitor converters with $V_{\text{ISO}} \leq V_{\text{H}}$ for at resonance operation.

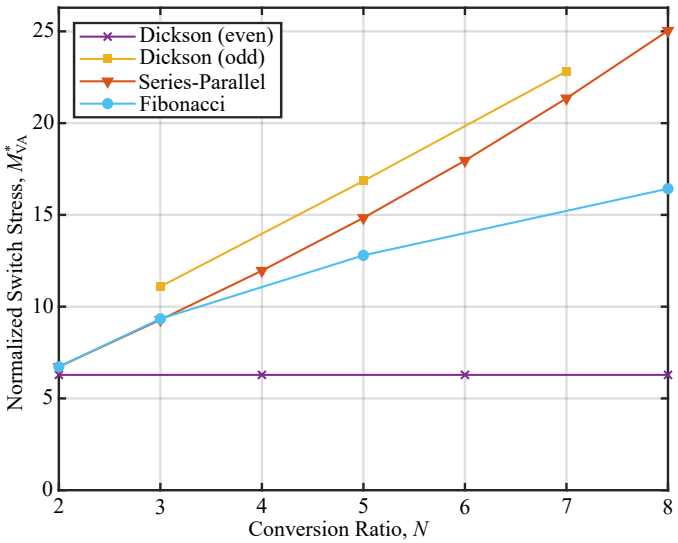


Fig. 12. Normalized switch stress, M^*_{VA}, versus conversion ratio, N, of capacitively isolated hybrid switched-capacitor topologies operating at resonance.

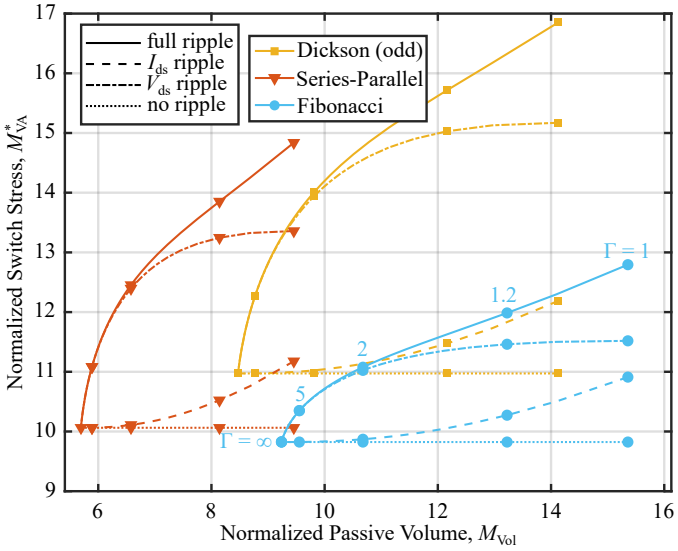


Fig. 13. Normalized switch stress, M^*_{VA}, versus normalized passive volume, M^*_{Vol}, for the odd Dickson, series-parallel, and Fibonacci converters at $N = 5$. The normalized switched stress is shown for no ripple, inductor ripple, capacitor ripple, and all ripple conditions at various values of Γ with zero isolation voltage.

work. The equation for normalized minimum passive volume [30] is expressed in (35) for convenience.

$$M^*_{\text{Vol}} = \frac{1}{\Gamma}\left(\frac{A_2}{2} + \sqrt{A_1\left(\frac{1}{4}A_3 + \rho B_1\right)}\right) \tag{35}$$

The passive volume of the presented capacitively isolated hybrid switched-capacitor converters as well as the even Dickson converter is shown in Fig. 10 as a function of the conversion ratio N for operation at and when feasible above resonance ($\Gamma \leq 3$) with zero isolation voltage. The series-parallel converter achieves the lowest passive volume across all conversion ratios. Furthermore, the overall passive volume can be greatly reduced when operating significantly above resonance. Above resonance operation reduces the sensitivity to component mismatch. Thus, the use of Class 2 multilayer ceramic capacitors (MLCC), which have higher energy density than Class 1 MLCCs, could further reduce the passive volume of the components presented in Fig. 10 [24].

The impact of isolation voltage on converter volume is shown in Fig. 11 for $V_{\text{ISO}} \leq V_{\text{H}}$. As expected, the minimum passive volume of a given converter increases with isolation voltage. The even Dickson converter experiences the greatest increase in minimum volume as all of the capacitors experience an increased dc voltage with higher isolation voltage.

B. Switch Stress

While there are many figure-of-merits for switch stress [35], a common one is the volt-amp (VA) product, which utilizes the

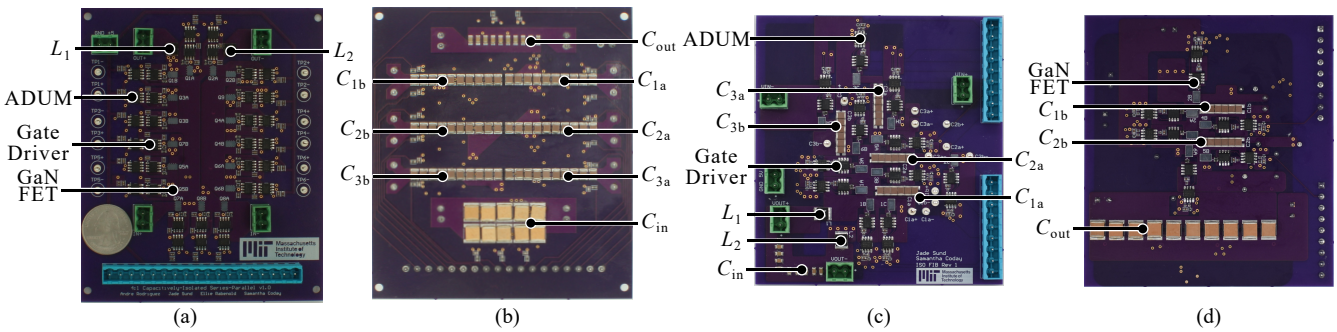


Fig. 14. Front (a) and back (b) sides of the hardware prototype of the 4:1 capacitively isolated series-parallel converter. Front (c) and back (d) sides of the hardware prototype of the 5:1 capacitively isolated Fibonacci converter.

product of voltage blocked and current conducted by a given switch to quantify the switch stresses [30], [36]. Typically, the peak voltage blocked is used in the VA product, but different switch current metrics (peak [36], average [32], [37], RMS [30]) are chosen by different works. This work utilizes the VA product expressed in (36) and the normalized VA product expressed in (37).

$$\mathrm{VA}_{\mathrm{tot}} = \sum_{k\in\{\mathrm{a,b}\}} \sum_{n=N_s} V_{\mathrm{ds,max},n}\ I_{\mathrm{RMS},n} \tag{36}$$

$$M^*_{\mathrm{VA}} = \frac{\mathrm{VA}_{\mathrm{tot}}}{V_{\mathrm{H}} I_{\mathrm{H}}} \tag{37}$$

The switch stress of the capacitively isolated even Dickson converter, and topologies of Fig. 4 is presented in Fig. 12. The even Dickson converter achieves significantly lower switch stress than those presented in this work as it has significantly reduced switch count at a given conversion ratio and the switches do not experience capacitor voltage ripple.

The tradeoff between switch stress and passive volume is summarized in Fig. 13 for $N = 5$. While the Fibonacci converter achieves low switch stress, particularly above resonance, it has the largest passive component volume. In contrast, the series-parallel converter has the lowest passive component volume, but incurs relatively high switch stress. The analysis presented accounts for the dc, capacitor ripple, and inductor voltage ripple components of Table III, but does not consider the increased switching losses associated with higher frequency switching. Furthermore, switching at resonance allows for ZCS and the presented analysis does not capture losses associated with not achieving ZCS. Consequently, the theoretical benefits in reduced switch stress indicated by Fig. 13 may not be achievable due to losses not incorporated by the VA rating. These insights are helpful for designers when considering application specific optimizations.

V. Hardware Verification

To validate the analysis, both a 4:1 capacitively isolated series-parallel converter and a 5:1 capacitively isolated Fibonacci converter were built. These prototypes are not intended to be direct comparisons; rather, they jointly validate the converter operation presented in Section III and provide design insights. Furthermore, the prototypes constitute testbeds and as such the components were selected to support at and above resonance operation within a reasonable frequency range ($f_{\mathrm{res}} \leq 200$ kHz) and were not optimized for power density. Both prototypes use the same components, listed in Table V with the exception of the inductor, which are from the same component family but have different values. For both converters, the normalized capacitance was chosen to be 1 μF.

Care was taken to minimize the commutation loops within switching cells as well as between contiguous switching devices for both prototypes. For the 4:1 capacitively isolated series-parallel converter prototype, shown in Fig. 14a and Fig. 14b, this resulted in a dual sided design which separates the switching cells from the power processing capacitors. For the 5:1 capacitively isolated Fibonacci converter prototype, shown in Fig. 14c and Fig. 14d, both sides of the board are used for switching and power paths. To reduce the commutation loop inductance of the Fibonacci converter hardware prototype, decoupling capacitance was added in parallel with $C_{2\mathrm{a}}$ and $C_{2\mathrm{b}}$. For both converters, signal and power isolation were achieved using ADUM5241s, though future implementations may employ bootstrapping methods to improve overall efficiency and to reduce board area [38].

All of the hardware discussed in this work was tested in an enclosure with high air flow. The efficiency measurements discussed in the following Section were conducted using a Yokogawa WT5000 Power Analyzer.

A. Series-Parallel Converter

The capacitor mid-range voltages shown in Fig. 15 at $V_{\mathrm{H}} = 100$ V and $f_{\mathrm{sw}} = 168$ kHz for the 4:1 series-

TABLE V
Components for the hardware prototypes.

Component	Part Number	Description
C	KEMET NP0	100 nF, 200 V
$L_{0_{\mathrm{SP}}}$	Würth 744384	600 nH, 3.2 mΩ, 21.5 A
$L_{0_{\mathrm{FIB}}}$	Würth 744384	1 μH, 5.8 mΩ, 15.8 A
S	EPC 2034	200 V, 8 mΩ
Gate Driver	NCP81074	5 V, 10 A
Isolator	ADUM5241	Power and Signal

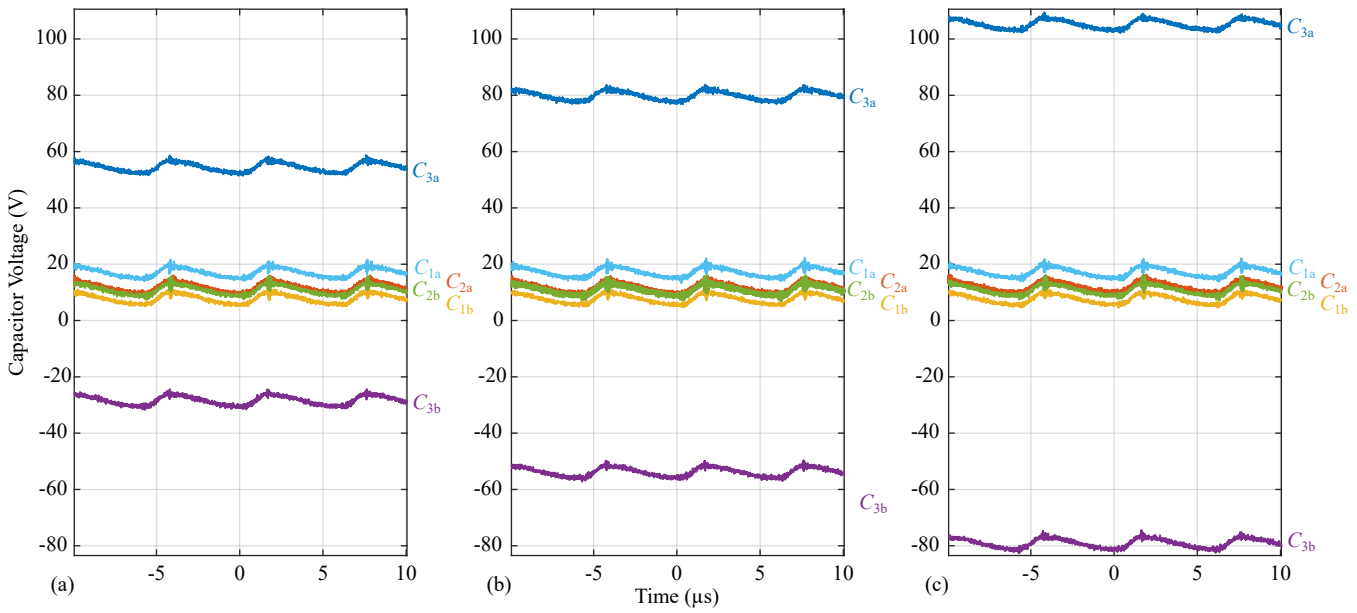


Fig. 15. Capacitor mid-range voltages for the 4:1 capacitively isolated series-parallel converter for (a) $V_{\text{ISO}} = 0$ V (b) $V_{\text{ISO}} = 25$ V (c) $V_{\text{ISO}} = 50$ V.

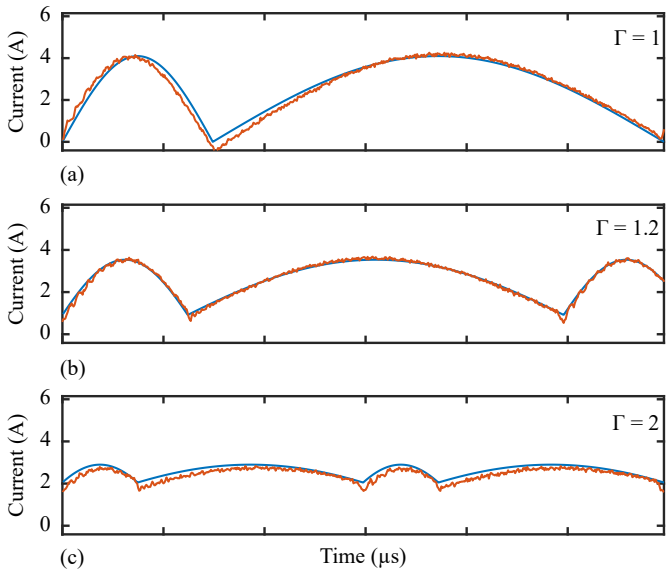


Fig. 16. Measured (orange) and calculated (blue) inductor current at $V_{\text{LO}} = 12$ V, $V_{\text{ISO}} = 0$ V, $P_{\text{out}} \approx 130$ W, and $f_{\text{sw}} = 168$ kHz for (a) $\Gamma = 1$, (b) $\Gamma = 1.2$, and (c) $\Gamma = 2$.

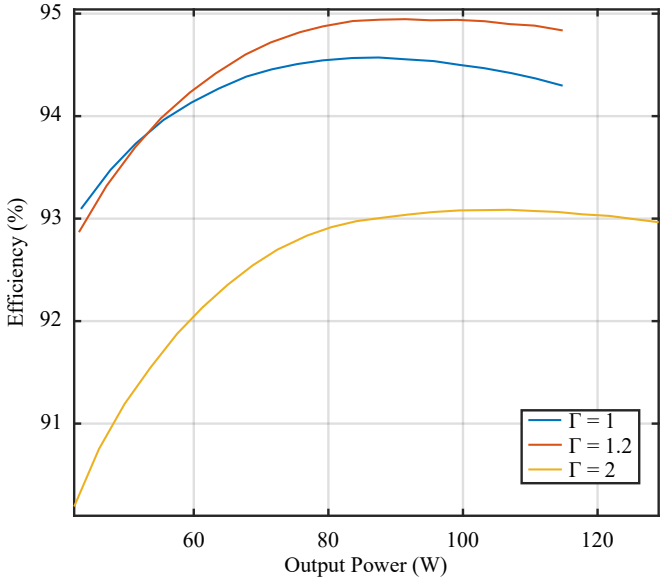


Fig. 17. Load sweep for the 4:1 capacitively isolated series-parallel converter operated at $V_{\text{H}} = 80$ V and $f_{\text{res}} = 120.2$ kHz for $\Gamma = \{1, 1.2, 2\}$.

parallel converter at selected isolation voltages confirm the analysis of Section III. Experimentally, the values of α_n for $n < \frac{N_c}{2}$ differ from the ideal of $\alpha_n = \frac{1}{2}$ due to component mismatch and layout asymmetries. The capacitor voltages split experimentally such that isolation voltage is only on capacitors $C_{3\text{a}}$ and $C_{3\text{b}}$; consequently, the voltages on the remaining capacitors are independent of isolation voltages as seen in Fig. 15. Furthermore, the capacitor voltage waveforms in Fig. 15 show soft-charging of the capacitors. The experimental inductor current waveforms in Fig. 16 show operation of the converter at and above resonance. The alignment of the derived inductor currents (blue) and the measured inductor currents (orange) in Fig. 16 provides initial validation of the inductor current analysis presented in Appendix A. Complete analytical validation of the inductor current is out of the scope of this work. However, the visible deviations between the expected and measured waveforms are expected due to error in frequency and load measurements used to develop the expected waveform. Slight deviation of the inductor current occurs with open loop control; thus, valley mode control may improve converter performance by ensuring ZCS. The series-parallel converter efficiency is shown in Fig. 17 for $V_{\text{H}} = 80$ V and $f_{\text{res}} = 120.2$ kHz for $\Gamma \in \{1, 1.2, 2\}$. Peak efficiency was measured of 94.9%, not including gate drive losses, was achieved at $\Gamma = 1.2$ for output powers between 87 W and 103 W. The peak at resonance efficiency was

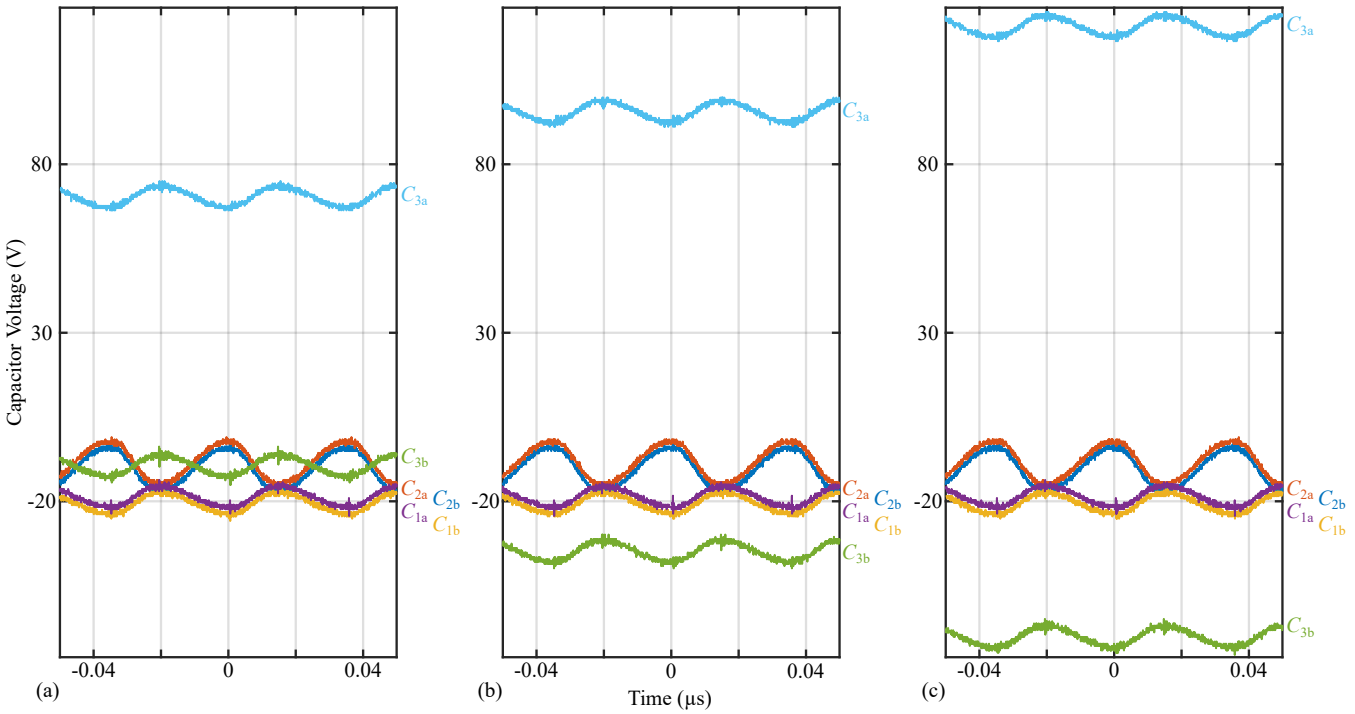


Fig. 18. Capacitor mid-range voltages for the 5:1 capacitively isolated Fibonacci converter for (a) $V_{\text{ISO}} = 0$ V (b) $V_{\text{ISO}} = 25$ V (c) $V_{\text{ISO}} = 50$ V.

94.5% for output powers between 75 W and 99 W. While operating at $\Gamma = 1.2$ increases the switching related losses compared to $\Gamma = 1$, the reduction in inductor ripple results in improved converter efficiency. Further increasing the switching frequency to $\Gamma = 2$, results in a decreased peak converter efficiency of 93% as the switching losses dominant the inductor losses. Thus, when at resonance converter operation is inductor loss dominant, operating slightly above resonance can provide efficiency improvements.

B. Fibonacci Converter

The capacitor-mid range voltages of Fig. 18 show that only C_{3a} and C_{3b} experience the isolation voltage further validating the mid-range voltage analysis.

Efficiency sweeps for the 5:1 Fibonacci converter were conducted under variable Γ for a fixed V_{ISO} shown in Fig. 20a and under variable V_{ISO} for a fixed Γ shown in Fig. 19. The converter efficiency, shown in Fig. 19 for $V_{\text{H}} = 100$ V and $V_{\text{ISO}} \in \{0\text{ V}, 25\text{ V}, 50\text{ V}\}$, is unaffected by the isolation voltage as the dc bias of the capacitors contributes to a small share of overall losses [39]. The efficiency for two 5:1 Fibonacci converters operated at $V_{\text{H}} = 80$ V for $\Gamma \in \{1, 1.2, 2\}$ is shown in Fig. 20a. While both converters are built using the boards seen in Fig 14c and Fig. 14d, component variation results in different resonant frequencies.

The converter with a lower resonant frequency achieves higher efficiency throughout, which indicates that the converter is switching loss dominated. For $\Gamma = 1$, the power processed was limited to 70 W for board one and 73 W for board two as at these power levels the switches began to reverse conduct. Thus, the maximum power processing capability of

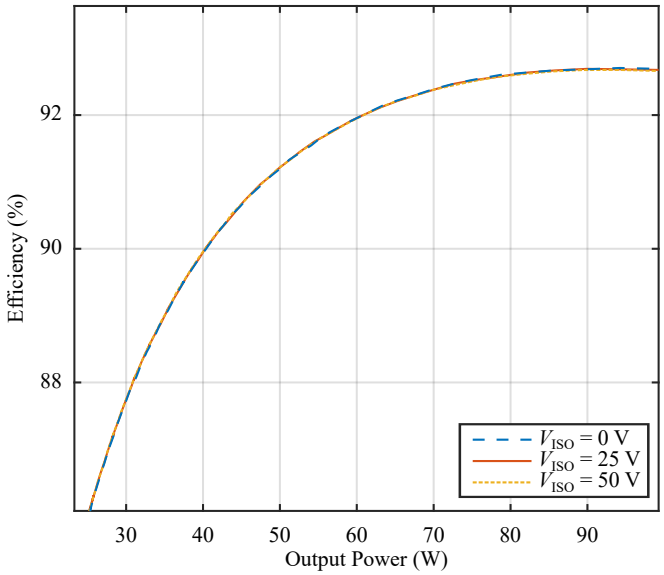


Fig. 19. An efficiency sweep for the 5:1 capacitively isolated Fibonacci converter operated $V_{\text{H}} = 100$ V and $f_{\text{sw}} = 141.5$ kHz at $V_{\text{ISO}} \in \{0\text{ V}, 25\text{ V}, 50\text{ V}\}$ and $\Gamma = 1$.

the converters was reached. Based on Table IV and the converter's operating conditions, the expected power processing capability of the converters was 65 W and 62 W for boards one and two respectively. The deviation between the observed and expected power processing capabilities may be due to losses not modeled by the theoretical power processing limits as well as the difficultly of accurately measuring C_0.

In addition, increasing the frequency from $\Gamma = 1$ to $\Gamma = 1.2$ theoretically increases the power processing capabilities of a

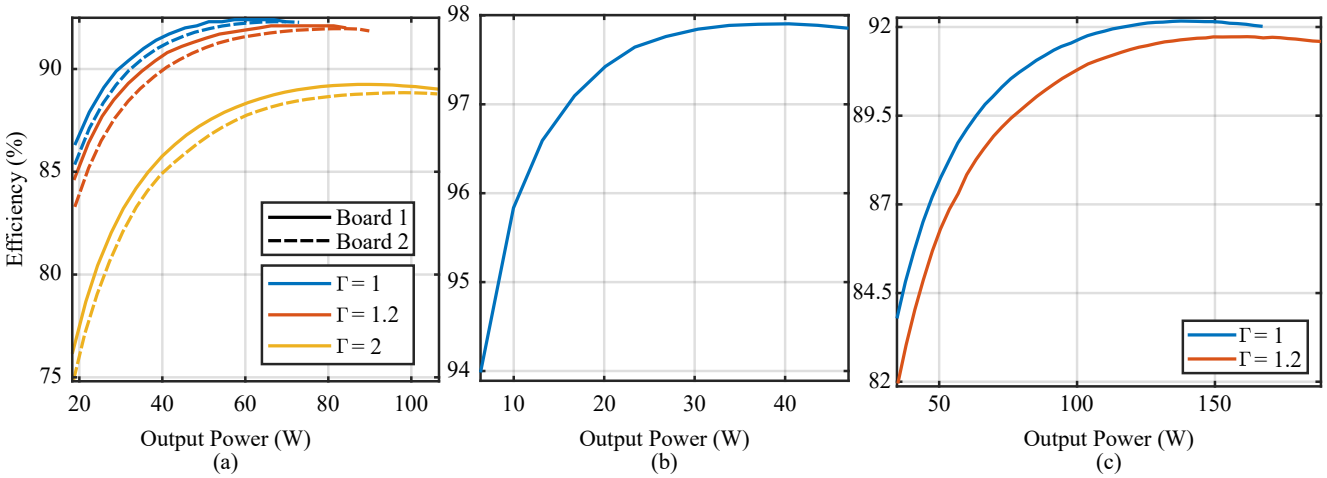


Fig. 20. An efficiency sweep for (a) two 5:1 capacitively isolated Fibonacci converter operated at $V_{\text{H}} = 80$ V, $\Gamma \in (1, 1.2, 2)$, and $V_{\text{ISO}} = 0$ V. Board one (solid lines) and board two (dashed lines) have resonant frequencies of $f_{\text{res}_1} = 153$ kHz and $f_{\text{res}_2} = 147.45$ kHz. (b) A buck converter operated at $V_{\text{IN}} = 32$ V, $D = 0.5$, and $f_{\text{sw}} = 75$ kHz. (c) A load sweep of a 12:1 SIPO converter composed of the two of (a) 5:1 capacitively isolated Fibonacci converters and the buck converter in (b) operating at a fixed 50% duty cycle.

given converter, which is observed experimentally in Fig. 20a. The maximum power processed shifts to 84.3 W for board one and 89.9 W for board two at $\Gamma = 1.2$. The theoretical maximum power processed were 78 W and 75 W for boards one and two respectively.

At resonance, the 5:1 Fibonacci converters achieve peak efficiencies of 92.3% and 92.4% before reaching the maximum power processed as constrained by switch voltage ripple. While operating above resonance ($\Gamma = 1.2$), provides a reduction in the converter efficiency (91.9%, 92.1%) it expands the range for which the maximum efficiency is achieved by reducing the capacitor ripple. The reduction in inductor current ripple did not improve converter efficiency, indicating that the converter is switching loss dominated at $\Gamma = 1$. Operation even further above resonance ($\Gamma = 2$) results in a decreased converter efficiency while increasing the power processing capability of the converter as the switch voltage ripple is significantly reduced.

C. Series-Input, Parallel Output Converter Architecture

One application for these capacitively isolated converters is in SIPO architectures such as those seen in Fig. 1. Typically, SIPO architectures for power converters experience higher efficiency at extreme conversion ratios then cascaded architecture and single converter approaches. In cascaded power converters, the total efficiency is a product of each converter in the series' efficiency as each converter still processes the total input power. Thus, cascading high efficiency converters can result in low overall efficiency. In contrast, for SIPO architectures the overall efficiency is weighted average of the voltage seen by each converter. The overall system efficiency as a function of the efficiency and input voltage of converter p and the total input voltage as expressed in (38).

$$\eta = \frac{\sum_p \eta_p V_{\text{in},p}}{V_{\text{in}}} \tag{38}$$

A SIPO architecture was developed as an extension of this work by stacking two 5:1 capacitively isolated Fibonacci converters on a regulating buck converter. The stacked 5:1 Fibonacci converters enforce an effective 10:1 conversion ratio, while ideally evenly sharing the power processed. A regulating buck converter was added which provides even further voltage conversion capabilities and enables the system to actively respond to input and load transients. The efficiency of the buck converter is characterized in Fig. 20b. For a desired output voltage V_{OUT}, the expected input voltages under balanced converter operation are $V_{\text{FIB},1} = V_{\text{FIB},2} = 5V_{\text{OUT}}$ and $V_{\text{Buck}} = V_{\text{IN}} - 10V_{\text{OUT}}$. For a desired output voltage of 15 V and a total system voltage of $V_{\text{IN}} = 192$ V, the expected per converter input voltages are $V_{\text{Buck}} = 32$ V and $V_{\text{FIB},1} = V_{\text{FIB},2} = 80$ V. To achieve this 12:1 conversion ratio the buck converter must operate at a 50% duty cycle.

The Fibonacci-based SIPO architecture was tested with an input voltage of 192 V. The experimentally determined input voltages were $V_{\text{Buck}} = 31.38$ V, $V_{\text{FIB},1} = 80.12$ V, and $V_{\text{FIB},2} = 80.5$ V. An efficiency sweep was conducted for the full converter at $\Gamma \in \{1, 1.2\}$ as shown in Fig. 20c. The Fibonacci-based SIPO architecture was capable of operating at an extreme conversion ratio of 12:1 while achieving a peak efficiency of 92.1%. The stacked architecture reaches a maximum power processed point of $P_{\text{OUT}} = 162$ W for $\Gamma = 1$ and $P_{\text{OUT}} = 188$ W for $\Gamma = 1.2$. Thus, the power processing capability of the stacked architecture is more than double that of an individual Fibonacci converter. Furthermore, the Fibonacci converters process $\approx 92\%$ of the total power and the Buck converter processes the remaining 8%.

VI. Conclusion

This work presents a systematic method for introducing isolation in existing inductor-at-the-output hybrid switched-capacitor converters derived from isolation techniques used in previous work [12]. Capacitively isolated variants of the series-parallel, odd Dickson, and Fibonacci converters were

presented and analyzed. A means of comparing the passive component volume of multi-inductor hybrid switched-capacitor converters was derived in Section IV and used to compare the topologies presented in this work. Section V provides validation of the capacitively isolated series-parallel and Fibonacci converters. Furthermore, the above resonance operation of this family of converters was validated. The Fibonacci converter was used to validate the stacked SIPO architecture as discussed in Section V.

APPENDIX

At $\Gamma = 1$, the inductor current can be defined as in (39), where $I_{\text{pk0},j}$ is the peak of the inductor current waveform at resonance as shown in Fig. 21. The phase shift $\theta_{0,j}$ is the relative phase shift between phases j and $j+1$ necessary to ensure continuity of current.

$$i_{L,j|\Gamma=1}(t) = I_{\text{pk0},j} \sin\left(\omega_j t + \theta_{0,j}\right) \tag{39}$$

As Γ increases above one, the minimum inductor current value increases, the maximum inductor current value decreases, and the average inductor current value remains the same and equal to the output current. This results in the convergence of the inductor current to the output current as $\Gamma \to \infty$. To determine an equation for inductor current as Γ increases above one, the inductor current can be expressed with a peak of $I_{\text{pk},j}$ a phase shift, θ_j, and dc offset, $I_{\text{v},j}$. Thus, the above resonance inductor current can be expressed as in (40).

$$i_{L,j}(t) = I_{\text{pk},j} \sin\left(\omega_j t \ + \ \theta_j\right) + I_{\text{v},j} \tag{40}$$

Figure 22 demonstrates the steps necessary to determine the inductor current above resonance. In Fig. 21a, the $\Gamma = 1$ inductor current is shown. The equations representing the inductor current in this figure are a piecewise function expressed in (41) in terms of (39). While Fig. 21 shows two phase operation, this analysis can be applied to multi-phase operation.

$$i_L(t) = \begin{cases} i_{L,1|\Gamma=1}(t) & \text{for } 0 < t < t_1 \\ i_{L,2|\Gamma=1}(t) & \text{for } t_1 < t < T_{sw} \end{cases} \tag{41}$$

As an example, moving from $\Gamma = 1$ to $\Gamma = 2$, the period is reduced by a factor of two. As such, the time durations, t_j, of each phase decrease by a factor of two. The half-wave resonant inductor current equation that satisfies these timing requirements is depicted by i_a in Fig. 22a. To simplify the inductor current analysis, i_a is phase shifted such that it can be expressed as i_b in (42).

$$i_b(t) = \begin{cases} i_a(t \ + \ \frac{\theta_1}{\omega_1}) & \text{for } 0 < t < \frac{t_1}{2} \\ i_a(t \ + \ \frac{\theta_2}{\omega_2}) & \text{for } \frac{t_1}{2} < t < T_{\text{sw}} \end{cases} \tag{42}$$

The phase shift is achieved by taking the difference of the at resonance and above resonance phase durations while a factor of $\frac{1}{2}$ maintains the symmetry of the sinusoid. An expression for θ_1 is presented in (43).

$$\begin{aligned} \theta_1 &= \omega_1\left(\frac{t_{1|\Gamma=1}}{2} - \frac{t_{1|\Gamma}}{2}\right) \\ &= \frac{\pi}{2} - \frac{\pi}{2\Gamma} \end{aligned} \tag{43}$$

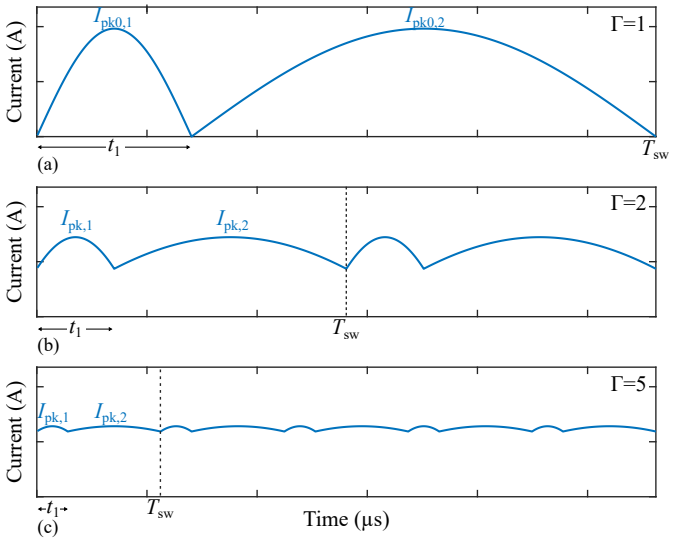


Fig. 21. Inductor currents for inductor-at-the-output converters operated at various values of Γ.

In addition to the phase shift, a vertical offset, I_{v}, is required to maintain a fixed average inductor current independent of Γ. A generalized equation for $I_{\text{v},j}$ in terms of the average inductor current at $\Gamma = 1$ and the average of the inductor current waveform without the vertical offset applied is shown in (44).

$$I_{\text{v},j} = I_{L,j|\Gamma=1} - \frac{1}{t_j}\int_{t_{j-1}}^{t_{j-1}+t_j} I_{\text{pk},j} \sin\left(\omega_j t + \theta_j\right)\, dt \tag{44}$$

In Fig. 22c, i_c shows the final inductor current with the phase and vertical offsets applied. This inductor current is equal to that of Fig. 21b. Using (40), the average inductor current can be expressed as in (45).

$$I_{L,j} = \frac{1}{t_j}\int_{t_{j-1}}^{t_{j-1} \ + \ t_j} I_{\text{pk},j} \sin\left(\omega_j t \ + \ \theta_j\right) + I_{\text{v},j}\ dt \tag{45}$$

The average output current can then be expressed as in (46).

$$I_{\text{out}} = \frac{\Gamma}{T}\sum_j \left(\int_{t_{j-1}}^{t_{j-1} \ + \ t_j} i_j(t)\ dt\right) \tag{46}$$

The charge through the inductor in phase j can be expressed as the integral of the inductor current (47).

$$\begin{aligned} q_j &= \int_{t_{j-1}}^{t_{j-1} \ + \ t_j} I_{\text{pk},j} \sin\left(\omega_j t \ + \ \theta_j\right) + I_{\text{v},j}\ dt \\ &= \frac{2I_{\text{pk},j}}{\omega_j} \cos\left(\omega_j t_{j-1} + \theta_j\right) \ + \ I_{\text{v},j}\left(\frac{\pi}{\omega_j \Gamma}\right) \end{aligned} \tag{47}$$

Evaluating the integral of (47) results in an equation for $I_{\text{pk},j}$, the amplitude of the inductor current waveform, in terms of the inductor charge flow and angular frequency of the phase (48).

$$\begin{aligned} I_{\text{pk},j} &= \frac{q_j\omega_j - I_{\text{v},j}(\frac{\pi}{\Gamma})}{2\cos\left(\omega_j t_{j-1} + \theta_j\right)} \\ &= \frac{q_{HI}\, H_{L,j}\, \omega_j - I_{\text{v},j}(\frac{\pi}{\Gamma})}{2\cos\left(\omega_j t_{j-1} + \theta_j\right)} \end{aligned} \tag{48}$$

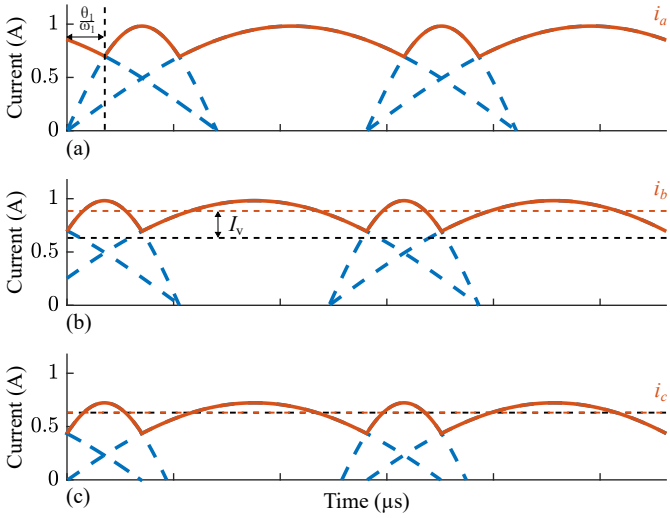


Fig. 22. Inductor current for operation above-resonance depicting necessary transformations to maintain a fixed dc output current at and above resonance. The orange curves represent the $\Gamma = 2$ waveforms.

Current continuity provides another expression for $I_{\text{pk},j}$ shown in (49).

$$\begin{aligned} &I_{\text{pk},j}\sin\left(\omega_j t_j + \theta_j\right) + I_{\text{v},j} \\ &\quad = I_{\text{pk},j+1}\sin\left(\omega_{j+1} t_j + \theta_{j+1}\right) + I_{\text{v},j+1} \end{aligned} \tag{49}$$

As all topologies considered in this work operate in two phases, further analysis will assume two-phase operation for simplicity. This could be extended to multiphase operation similarly to the method in [30]. The average inductor current per phase is equal to the charge for each period divided by the respective period duration. The average current in each phase can therefore be expressed as shown in (50).

$$\frac{I_{L,1}}{I_{L,2}} = \frac{H_{L,1}\omega_1}{H_{L,2}\omega_2} \tag{50}$$

The right hand side of (50) can be evaluated using Table II for all topologies presented in this work. Note that when $\frac{H_{L,1}\omega_1}{H_{L,2}\omega_2} = 1$, the average currents and consequently the vertical offsets, $I_{\text{v},1}$ and $I_{\text{v},2}$, and inductor current peaks, $I_{\text{pk},1}$ and $I_{\text{pk},2}$ are equal.

With $I_{\text{v},1} = I_{\text{v},2} = I_{\text{v}}$, (48) and (49) can be simplified to express the ratio of $I_{\text{pk},1}$ to $I_{\text{pk},2}$ as seen in (51).

$$\begin{aligned} \frac{I_{\text{pk},1}}{I_{\text{pk},2}} &= \frac{\cos\left(\frac{\omega_2}{\omega_1}\frac{\pi}{\Gamma} + \theta_2\right)}{\cos\left(\theta_1\right)} \\ &= \frac{\sin\left(\frac{\omega_2}{\omega_1}\frac{\pi}{\Gamma} + \theta_2\right)}{\sin\left(\frac{\pi}{\Gamma} + \theta_1\right)} \end{aligned} \tag{51}$$

Since the inductor current in each phase starts and ends at the same value and the waveform is half-wave symmetric, the identities presented in (52) may be used.

$$\begin{aligned} \sin\left(\theta_1\right) &= \sin\left(\frac{\pi}{\Gamma} + \theta_1\right) \\ \cos\left(\theta_1\right) &= -\cos\left(\frac{\pi}{\Gamma} + \theta_1\right) \end{aligned} \tag{52}$$

Therefore, using (52), (51) can be solved for the relationship between θ_1 and θ_2 expressed in (53).

$$\theta_1 = \theta_2 + \frac{\omega_2}{\omega_1}\frac{\pi}{\Gamma} \tag{53}$$

Equations (51), (52), and (53) show that the peak inductor currents are equal: $I_{\text{pk},1} = I_{\text{pk},2} = I_{\text{pk}}$. The dc offset term $I_{\text{v},j}$ can be solved for using the capacitor and inductor voltage ripple. The voltage ripple of the effective inductance, $L_{\text{eff},j}$ is expressed in (54).

$$\Delta v_{L,j} = 2L_{\text{eff},j} I_{\text{pk}} \omega_j \cos\frac{\pi(\Gamma - 1)}{2\Gamma} \tag{54}$$

The capacitor voltage ripple of the per phase effective capacitance $C_{\text{eff},j}$ is expressed in (55).

$$\Delta v_{C,j} = \frac{2I_{\text{pk}}}{\omega_j C_{\text{eff},j}} \cos\frac{\pi(\Gamma - 1)}{2\Gamma} - \frac{I_{\text{v}} t_j}{C_{\text{eff},j}} \tag{55}$$

KVL dictates that these ripples must be equal; thus, using (54), (55), and (56), it can determined that $I_{\text{v}} = 0$.

$$\omega_j = \frac{1}{\sqrt{L_{\text{eff},j} C_{\text{eff},j}}} \tag{56}$$

Parameter I_{pk}, can then be determined from (48) as shown in (57).

$$I_{\text{pk}} = \frac{q_{HI}\, H_{L,j}\, \omega_j}{2\cos\left(\omega_j t_{j-1} + \theta_j\right)} \tag{57}$$

$$= \frac{\pi I_{\text{out}}}{2\Gamma\cos\left(\frac{\pi(\Gamma-1)}{2\Gamma}\right)} = \frac{\pi I_{\text{out}}}{2\Gamma\sin\left(\frac{\pi}{2\Gamma}\right)} \tag{58}$$

Expressions for inductor currents $i_{L,1}$ and $i_{L,2}$ in terms of I_{out} and as a function of Γ are shown in (59) and (60), respectively.

$$i_{L,1}(t) = \frac{\pi I_{\text{out}}}{2\Gamma\sin\left(\frac{\pi}{2\Gamma}\right)} \sin\left(\omega_1 t + \frac{\pi\,(\Gamma - 1)}{2\Gamma}\right) \tag{59}$$

$$i_{L,2}(t) = \frac{\pi I_{\text{out}}}{2\Gamma\sin\left(\frac{\pi}{2\Gamma}\right)} \sin\left(\omega_2 t + \frac{\pi\,(\Gamma - 1)}{2\Gamma} - \frac{\omega_2 \pi}{\omega_1 \Gamma}\right) \tag{60}$$

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